



Five Day Technology Workshop

on

Optimizing Performance of Parallel Programs on Emerging Multi-Core Processors & GPUs (OPEGC-2009)

Dates: June 1-5, 2009,

Venue : Indian Institute of Technology Madras, Chennai

Topic: Performance of Compression Algorithms on Multi-core Processors (Cell Processors)

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The speed of compression and decompression is critical in computing, because sending the data directly will be preferable if the overhead of compression is high. There has been much work performed on floating point compression. Several algorithms that provide fast compression, even though the compression achieved is less than that of popular compression algorithms are becoming popular. Bandwidth limitations are a bottleneck in several applications on Multi-Core Processors. These limitations may be (i) memory bandwidth, especially on multi core processors (ii) network bandwidth in MPI applications (iii) Bandwidth to disk in I/O intensive applications or (iv) WAN bandwidth in remote sensing applications that send observational data to a central site. Fast compression of floating point numbers can ameliorate bandwidth limitations. Here, it is crucial for the speeds of compression and decompression to be greater than the bandwidth. Otherwise, it will be faster to send the data directly. We have carried out experiments the effectiveness of a simple Stride based Compression Algorithm to deal with this problem, on the CellBE processor. We find that our approach is not fast enough for dealing with the memory bandwidth limitations. However, it can be effective in dealing with the other three limitations. Our efforts are focused on evaluate the potential of this approach on the Cell Processor.

We have investigated the effectiveness fast floating-point compression in ameliorating different types of bandwidth limitations. Our result indicate that this proposal that this approach would not be effective in dealing with main memory bandwidth limitations. In future work, we wish to improve the compression algorithm used, so that we obtain good compression on a greater variety of applications. It will also be useful to evaluate its effectiveness in other types of architectures, such as GPUs, and also on the latest generations of cell blades. The Cell processor contains a PowerPC core, called the PPE, and eight co-processors called SPEs. The SPEs are meant to handle the bulk of the computation bottleneck. They have a combined peak speed of 204.8 GFlops/s in single precision. Each SPE is capable of sending and receiving at 25.6 GB/s.

Ref: *Fast Floating Point Compression on the Cell BE Processor;* T.V. Sivakumar, P.K. Baruah Ashok Srinivasan