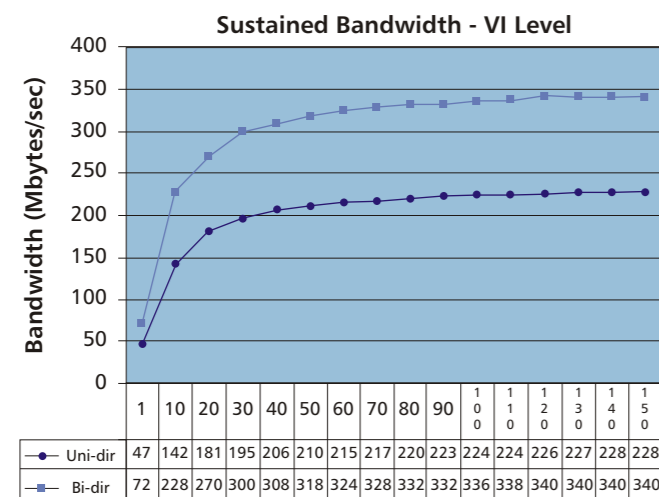
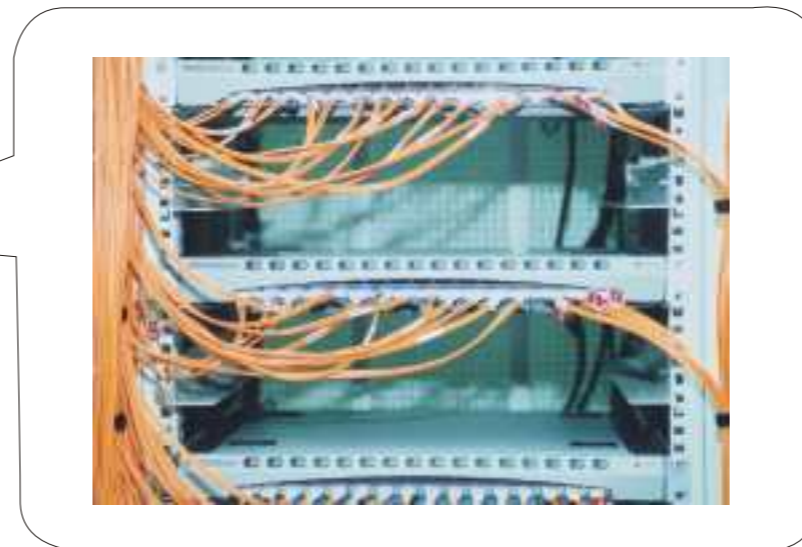


PARAMNet-II has been designed taking into consideration very high reliability requirements of the end users. Rigorous design validation cycles on pre-production run and burn in practices during the manufacturing, assures users of a highly reliable and stable product.

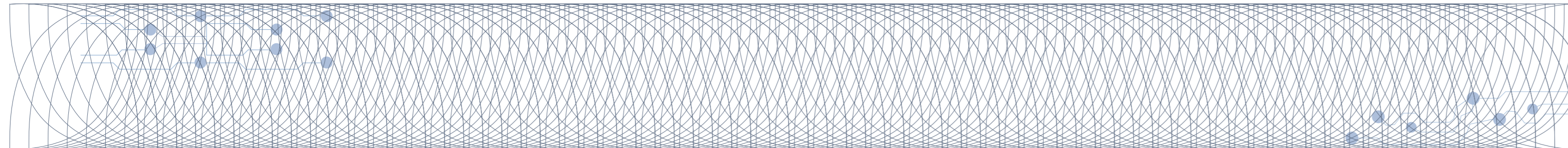
Quality practices conform to the ISO standards. The hardware components have monitoring features to quickly detect any problems. It is possible to design fault tolerant clusters to provide greater reliability to the end users.



Message Size (Kbytes)



PARAMNet-II Rack interconnecting 64 Compute Nodes of PARAM Padma cluster.



### SPECIFICATIONS

#### SAN Switch (SANSW8/SANSW16)

Number of Ports	8/16
Link Physical Layer	2.5 Gbits/Sec: Fiber opticlink
Switch Architecture	Non-blocking Crossbarbased Architecture
Latency	0.5 Microsecond
Bandwidth	230 Mbytes/Secfull duplexper port
Dimensions	1U 19" Rack Mountable [(0.044m (H))x 0.435m (W) x 0.512m (D)]
Power	100W: 120/240VAC



#### PARAMNet-II NIC

Host Interface	PCI 2.2: 64 bit/66MHz
Link Physical Layer	2.5 Gbits/SecFiber opticlink
Latency	10 Microseconds
Bandwidth	Aggregate > 300 Mbytes
Protocols	VIA, AM
OS Support	AIX/LINUX/SOLARIS/WINDOWS
Communication & Libraries	C-MPI (MPI 1.2Compatible)
Dimensions	Short PCI Card Format(0.175m x 0.125m)
Power	< 15W



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# PARAMNet-II

## High Performance System Area Network



Centre for Development of Advanced Computing

[www.cdacindia.com](http://www.cdacindia.com)

C-DAC has forged its decade of hardware technology development expertise, in the state-of-the-art areas of VLSI Design, High Speed Networking and Digital System Design to develop the next generation high performance System Area Network (SAN), PARAMNet-II, with speeds of 2.5 Gbits/Sec full duplex supporting multiple software interfaces like Virtual Interface Architecture (VIA) and Active Messages (AM). PARAMNet-II, with ultralow latency & high bandwidth, offers the best price/performance ratio for interconnecting High Performance Clusters of Workstations, Servers, Personal Computers and Single Board Computers.

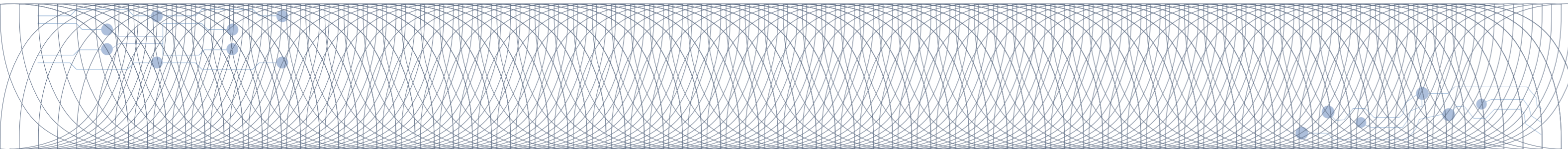
PARAMNet-II is the prime interconnect fabric for connecting Compute Nodes, File Servers and Graphics Nodes in C-DAC's range of parallel computing systems & most recent in the series, PARAM Padma, a parallel supercomputing system with a peak computing power of One Teraflop. It is one of the most powerful supercomputers developed and deployed for High Performance Scientific and Business Computing Applications in the Asia Pacific Region.

#### FEATURES

- ▶ Ultra low latency and high bandwidth
- ▶ Non-blocking configuration allows multilevel switches to control upto 1024 compute hosts
- ▶ VIA standard compatible
- ▶ Diverse platform support AIX / Solaris / Linux / Windows
- ▶ Mechanically compact Switch with ultra-thin chassis
- ▶ Highly scalable

#### PARAMNet-II COMPONENTS

- SAN Switch (SANSW 8/SANSW 16)
- PARAMNet-II Network Interface Card (NIC)
- C-DAC's Virtual Interface Provider Library (C-VIPL)



#### PARAMNet-II Network Interface Card (NIC)

The PARAMNet-II NIC is based on C-DAC's Communication Co-Processor-III (CCP-III) chip.

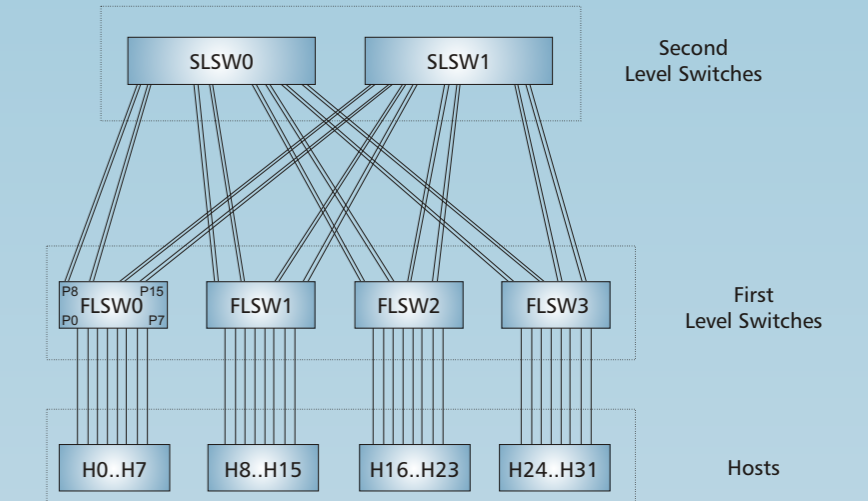
- Interfaces to SANSW8 (8 port) and SANSW16 (16 port) PARAMNet-II switch
- Supports 2.5Gbps (fibre) links
- Host interface PCI 2.2 64bit/66MHz
- Support for connectionless and connection oriented protocols. Configurations available for VIA (connection oriented) and AM (connectionless) protocols. Can be configured for other protocols
- Capable of performing I/O from paged virtual memory
- Supports different page sizes
- Support upto 512MB (128k pages) of dynamically registered communication buffers
- Support upto 1024 connections and upto 1024 completion queues
- Hardware implementation of Doorbells, Protection Mechanism, Address Translation, etc. and specialized instruction set of the co-processor for low latencies
- Direct user level hardware access with protection
- Packetization and re-assembly of messages done in hardware
- Error detection and recovery done in hardware
- Latency of 10 microseconds approximate
- Aggregate Bandwidth in excess of 300 Mbytes/Sec



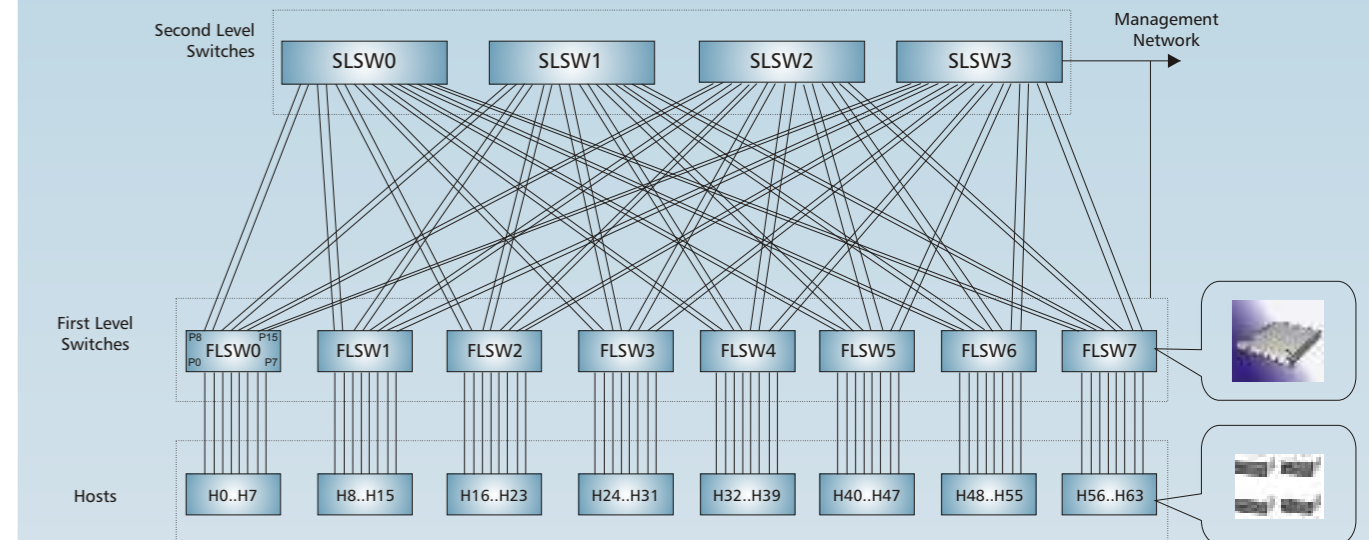
#### PARAMNet-II SCALABILITY

A single switch can support up to eight (SANSW8) or sixteen (SANSW16) hosts. To support more hosts, a multistage network can be configured. The switch can be used to build various network topologies.

PARAMNet-II network comprises of N hosts connected in non-blocking fat tree topology. For more than eight/sixteen hosts, multiple SANSW8/SANSW16 switches are assembled.



Block diagram of 32-hosts, using six SANSW16 switches

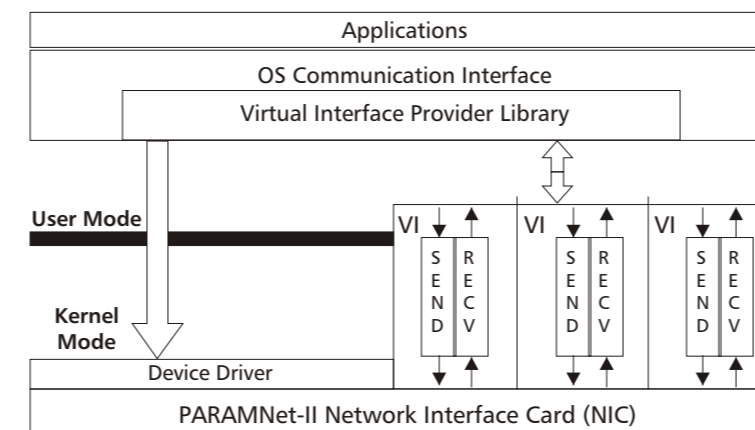


Block diagram of 64-hosts, using twelve SANSW16 Switches

As the switch latencies are very low, the multiple levels of switches as shown in the above figures would have very little overheads. Thus it is possible to build similar larger non-blocking configurations using SANSW8/SANSW16 switches without performance degradation.

#### C-DAC's Virtual Interface Provider Library (C-VIPL)

An application programming interface for PARAMNet-II.



- Adheres to VIA Specification Version 1.0 (jointly authored by Intel, Compaq and Microsoft)
- Thread Safe Implementation
- Support for diverse Operating Systems: AIX, Linux, Solaris and Windows
- Compatible with C-DAC-MPI (C-MPI) and Public domain MPI (MPICH) of Argonne National Lab and Mississippi State University.

C-VIPL is a part of KSHIPRA, scalable communication substrate for Cluster of Multiprocessors designed to support low latency, high bandwidth and high level of aggregate system performance.

#### SAN Switch (SANSW 8/SANSW 16)

- Non-blocking crossbar-based architecture
- 8/16-ports providing 2.5 Gbps, full duplex raw bandwidth per port (2 Gbps, full duplex data bandwidth)
- Low latency (~0.5 microseconds) and high bandwidth (~230 Mbytes/sec) full duplex per port
- Distributed schedulers allow individual routing tables per port, also allowing for any network topology (native support for CLOS topology)
- Virtual channel based routing with 1KB of buffering per port each at input and output
- Interval routing scheme based on 32-bit header (16-bit routing information)
- Group adaptive routing based on LRU algorithm to ensure uniform bandwidth distribution in a group
- Point-to-point flow control with pause and resume tokens
- More than 8/16 ports are supported using multi-level switching for very large clusters
- Uses state of the art VCSEL optical transceivers with low cost cabling (850 nm, multimode fiber)
- Ethernet (10Mbps) based management interface allows for remote access and control of multiple switches
- Compact mechanical dimensions (19" rack mountable) with ultrathin chassis (1U height)

