

# Migrating FPGA based PCI Express Gen1 design to Gen2

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## Abstract

*PCI Express (Peripheral Component Interconnect Express) abbreviated as PCIe or PCI-E, is designed to replace the older PCI, PCI-X, and AGP standards. PCIe 2.1 or Gen2 is the latest standard for expansion cards that has come recently on mainstream personal computers. The designer can implement PCIe inside an FPGA by either developing the complete PCIe protocol or by purchasing a readily available IP from the market. Different solutions for the implementation of PCIe design using FPGAs are available through couple of vendors, including Xilinx and Altera. Xilinx has Soft IP as well as Hard IP available to the designer to get started with the design. In this paper we present our implementation of PCIe Gen1 design in various families of Xilinx devices and further show the migration of PCIe Gen1 design to Gen2 design using state of the art FPGAs. We also highlight our interfacing logic design consideration for the Gen1 and Gen2 IP blocks and some of the critical aspects that needs to be addressed while designing the board.*