

# Automated functional verification engine for 10Gbps Network switch

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## Abstract

*We have developed a proprietary 10Gbps switching architecture for HPC market. Being proprietary, it is not compliant to standard protocol verification suits. Due to its large port count, we needed a scalable, reusable and user friendly automated functional verification engine. This could not be HDL based for three reasons viz. scalability, large memory footprint and simulation speed.*

*In this paper, we describe a SystemC verification model with few other VHDL components to meet our validation requirement. This engine can generate different types of test packets to exercise all possible packet routing paths within the switch. Directed as well as random tests simulate stressful traffic patterns, to validate congestion management across all ports. Simple user-control file facilitate user to configure and club various test cases in a single run. System statistics are logged for analysis of switch behavior.*

*We could achieve real time simulation speed improvement and scale the engine to validate multiple ports simultaneously. Results were encouraging compared to a dual port VHDL analyzer designed earlier and found to have speedup up to 1.5 times. Analysis of test results was effective due to organized output file. In future, we plan to include latency and bandwidth calculations along with performance graphs.*