International workshop on RISC-V for HPC (RISCV-HPC)

17th December 2025, Hyderabad – India

Technical Program

Time	Session		Presenters
13:55 – 14:00	Welcome Note		RISCV-HPC Organizing Committee
14:00 – 14:40	Keynote #1		
14:40 – 15:00	Paper Session 1	Hardware-Software Co-Design of Post-Quantum FALCON Digital Signature Scheme with RISC-V	Rishabh Shrivastava and Utsav Banerjee, IISC Bangalore
15:00 – 15:20		Neuromorphic Adaptive Precision RISC-V Processor with Real-Time Precision Scaling and Neuronal State Management	Om Maheshwari, Sahil Maurya and Dr. Bikram Paul, IIT Mandi
15:20 – 16:00	Tech Talks		CaligoTech, C-DAC, Vyoma Systems
16:00 – 16:30	Break		
16:30 – 17:10	Keynote #2		
17:10 – 17:30	Paper Session 2	Performance Evaluation of AI Inference on the Tenstorrent Wormhole RISC-V Accelerator	Kishor Yerol Damodaran, Abhishek Patel, Krishnan Gopal Gupta, Shashank Sharma, Samrit Kumar Maity and Sanjay Wandhekar, C-DAC
17:30 – 17:50		Porting an Enterprise Linux Distribution to Custom RISC-V Hardware: A Rocky Linux Case Study	Surendra Billa, Rushikesh Jadhav, Rutuja Sandbhor, Yogeshwar Sonawane and Sanjay Wandhekar, C-DAC
17:50 – 18:10		Quantitative Evaluation of Hazard Mitigation Strategies in a 5-Stage RISC-V Pipeline: A Benchmark-Driven Analysis Using Fibonacci and Prime Sieve	Kushagra Agrawal, Anindita Basak, Abhishek Raj and Aakarsh Singh, KIIT
18:10 – 18:20		Performance Analysis of Compiler Code Generation for HPC and AI Kernels on RISC-V	Rama Kishan Malladi and Nitya Hariharan, Tenstorrent
18:20 – 18:30		RISC-V Based SoC Design Featuring Fixed and Floating Point Units with Integrated FFT Accelerator for DSP Workloads	Umer Kudachi, Shreevatsa Alawandi, Aishwarya Beedanal and Dr. Saroja Siddamal, KLE Technological University