techzine

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INSPIRING INSIGHTS ON NEW FRONTIERS | IDEAS TO ACTION | PROGRESS PULSE: A PERFORMANCE DASHBOARD | TECH ROLL-OUTS | INTERNATIONAL OUTREACH | EVENTS | BACK-END SQUAD

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Message from **Director General**

I am pleased to announce the release of the Eighth Issue of Techzine R&D Digest from C-DAC. Heartfelt congratulations to the Corporate R&D team on this significant achievement. I extend my warmest greetings to all C-DACians who have contributed in Techzine for sharing their expertise, passion for research, innovation, and the pursuit of knowledge.

This issue is focusing on various aspects of "Indigenous Microprocessor Development". As you all are aware that C-DAC has played a pivotal role in Digital India RISC – V (DIR-V) program of MeitY, contributing across the entire value chain—from microprocessor design and verification to ecosystem development and national deployment. As a part of the same, C-DAC has developed the VEGA series of RISC-V processors, targeting applications from embedded systems to high-performance computing.

I urge all C-DACians to proliferate the usage of VEGA processor for various projects/solutions being implemented by C-DAC.

Magesh Ethirajan

Message from **Editorial Board**

The Editorial Board is delighted to reflect on the substantial impact of past seven issues of Techzine in advancing the research and development landscape of C-DAC. These editions have effectively highlighted the pioneering innovations, facilitating their recognition, deployment, and adoption across the key ministries including MeitY as well as in academia, research institutions, industries, and among other vital stakeholders.

We are proud to present the Eighth Issue of Techzine, focusing on the theme: "Indigenous Microprocessor Development." This issue features special articles on “ChipIN Centre – Catalysing India's Chip Design Revolution”, highlighting a critical initiative shaping the nation's semiconductor ecosystem and “Indigenous HPC Processors and AI/ML hardware accelerators” providing C-DAC's pivotal role in high-impact technology domains.

Each edition of Techzine serves as a celebration of the remarkable achievements of C-DACians across all centers. We extend our heartfelt gratitude to our esteemed contributors and readers for their continued support, enthusiasm, and engagement.

As we turn the page to this new chapter, we look forward to journeying ahead with you, exploring and celebrating the spirit of innovation that defines C-DAC.

INSPIRING INSIGHTS ON NEW FRONTIERS

ChipIN centre – CATALYSING INDIA'S CHIP DESIGN REVOLUTION

Shri Vivian Desalphine
Scientist F
C-DAC Bangalore

Introduction

India is undergoing a pivotal transformation in semiconductor design and innovation. At the forefront is ChipIN Centre, at C-DAC Bangalore, a national hub created to empower students, faculty, startups, and MSMEs to move from concept to chip. This initiative is a cornerstone in India's ambitious journey to achieve self-reliance in semiconductor domain.

With semiconductors forming the core of modern electronics—from mobile phones and electric vehicles to medical devices and space systems—developing domestic capabilities is no longer a choice but a necessity. Strategic initiatives like Digital India, Make in India, and the India Semiconductor Mission (ISM) are creating a framework where innovation thrives, and India emerges not only as a consumer but also as a global contributor to chip design.

Two flagship programmes under MeitY are driving this change: Chips-to-Startup (C2S) and Design Linked Incentive (DLI). Both converge at ChipIN Centre, which provides shared access to industry-grade Electronic Design Automation (EDA) tools, fabrication support, enablement of packaging, and post-silicon validation. It bridges the gap between ideas and silicon, enabling thousands of students, researchers, and entrepreneurs across India to dream, design, and deliver world-class chips.

ChipIN centre – CATALYSING INDIA'S CHIP DESIGN REVOLUTION

Chips-to-Startup (C2S) Programme – Building a Talent and Innovation Pipeline

Chips-to-Startup (C2S) Programme is a national initiative launched by Ministry of Electronics and Information Technology (MeitY) to build a strong foundation for chip design and innovation in India. It is the third phase of Special Manpower Development Programme (SMDP), which helped set up VLSI (Very Large-Scale Integration) design labs in engineering colleges and universities across the country. C2S Programme is taking this effort to the next level by aiming to generate 85,000 trained students and researchers over five years in cutting-edge semiconductor design technologies.

The programme currently supports over 260+ academic institutions, startups/MSMEs working on innovative chip design and embedded systems projects. The focus is on hands-on learning and real-world applications—students and researchers are given access to industry-grade EDA tools, design platforms, and chip fabrication and prototyping services through ChipIN Centre.

Some key highlights of C2S Programme include:

- Generation of 85,000 specialized manpower in chip design and embedded systems.
- Development of over 175 ASICs, 30 FPGA-based systems, and 20 full system-level solutions.
- Incubation of 25 startups and facilitation of 10 technology transfers.
- Access to SmartLab facilities and centralized EDA design tools and services through ChipIN Centre
- A growing number of patents and research publications from participating institutions

In short, C2S is not just about learning—it's about designing real chips, solving real-world problems, and creating a vibrant ecosystem of future-ready talent and innovation in semiconductors.

Design Infrastructure Support (DIS) under DLI Scheme – Accelerating Startup Innovation

To strengthen India's chip design ecosystem, the Design Linked Incentive (DLI) Scheme was launched by MeitY. One of its key components, Design Infrastructure Support (DIS), helps domestic startups and MSMEs by giving them access to high-end chip design EDA tools and services that are otherwise expensive and hard to obtain.

Through ChipIN Centre at C-DAC Bangalore, startups can access industry-grade EDA tools from global vendors. These tools are hosted centrally at ChipIN Centre, allowing secure and efficient remote access. This removes the need for costly infrastructure and lets startups focus on design and innovation.

Beyond tools, DIS has enabled access to the following services for startups:

- Multi-Project Wafer (MPW) prototyping
- IC packaging
- Post-silicon validation
- Foundry access and PDK support

ChipIN centre – CATALYSING INDIA'S CHIP DESIGN REVOLUTION

These services are provided through expert partners identified via a national-level Expression of Interest (EOI). Startups also have the flexibility to choose other capable vendors based on their specific project needs.

Already, over 72 chip design projects from 69 Indian startups and MSMEs have been supported under DIS. These projects span various technology domains. This support is helping Indian startups bring their chip designs to life faster, reduce time-to-market, and compete globally.

DIS under DLI Scheme is more than infrastructure, it's a launchpad. Several startups under the scheme have reached tape-out, are filing patents, securing investor interest, and preparing to bring indigenous semiconductor products to the global stage.

ChipIN Centre – National Infrastructure for Chip Design

At the core of India's semiconductor design effort is ChipIN Centre, at C-DAC Bangalore. It is the country's national-level grid for EDA tools, supporting large-scale chip design by students, researchers, startups, and MSMEs. EDA tools are specialized software used to design, simulate, and verify integrated circuits (ICs). These tools are essential in chip-making but are expensive and require advanced computing infrastructure. ChipIN Centre addresses this challenge by offering centralized, remote access to world-class EDA tools—enabling users across India to work with the same tools used by global chip design companies.

Hosted at C-DAC Bangalore, ChipIN Centre supports one of the largest collections of EDA tools globally, including tools from Cadence, Synopsys, Siemens EDA, Ansys, Keysight, and Xilinx. It also provides access to Param Utkarsh Supercomputing Facility, allowing institutes and startups to securely log in and carry out chip design, simulation, and verification without the need to invest in their own infrastructure. Access to the IBM OpenPOWER Microwatt core and its complete design flow is also made available on Param Utkarsh, enabling students and startups to explore advanced processor-level design using EDA tools and design workflows. This integrated environment helps users move confidently from RTL to GDSII, building real-world skills and accelerating innovation.

ChipIN goes far beyond tools. It also enables:

- Multi-Project Wafer (MPW) services for chip prototyping, both in India (SCL foundry) and through global foundries.
- Fab compliance checks to ensure chips meet manufacturing standards for fabrication at SCL
- Enablement of post-silicon validation to test fabricated chips.
- FPGA-based prototyping, with boards distributed to over 100 academic institutions.
- SmartLab facility for hands-on exposure and experimentation.

By making this infrastructure widely available, ChipIN Centre is removing barriers and democratizing chip design in India. This is not just about supporting individual projects—it is about building a self-reliant semiconductor design ecosystem. With every trained student and every chip designed, India moves closer to becoming a global innovation leader in semiconductor domain.

ChipIN centre – CATALYSING INDIA'S CHIP DESIGN REVOLUTION

ChipIN Centre – Creating Impact Nationwide

India's growing ambitions in the semiconductor sector are backed not just by policy and funding, but also by enabling infrastructure that makes chip design truly accessible. ChipIN Centre is not just a facility, it's a movement that's helping democratize chip design and innovation across the country. From the snow-covered campuses in Jammu and Kashmir to the coastal institutes of Tamil Nadu, and from startups in remote corners of the North-East to top-tier research institutes in metros—ChipIN Centre is reaching and enabling everyone. Through centralized infrastructure, expert support, and remote access to world-class EDA tools, the Centre is breaking down barriers that once limited semiconductor innovation to a select few.

In the past, access to chip design tools and facilities was limited to a handful of elite institutions and large companies. The high cost of EDA tools, limited access to fabrication services, and the lack of infrastructure in many colleges and startups made it difficult for talent to thrive. ChipIN Centre is changing that equation.

By hosting EDA tools on a national grid and enabling secure remote access, ChipIN is ensuring that even small engineering colleges in tier-2 and tier-3 cities can train students in the latest chip design methodologies. Over 260 academic institutions are accessing EDA tools from the national EDA tools grid, and many more are being onboarded. Students from rural regions are now able to use the same tools as global chip designers—without leaving their campus. This access has not only improved learning outcomes but has also inspired students to design real chips and file patents, setting the stage for India's next generation of semiconductor innovators.

Startups are the heartbeat of innovation, and in the chip design space, they are often the bold risk-takers building niche, high-tech solutions. But without access to design infrastructure, their journey is full of hurdles. Through the DIS under DLI Scheme, ChipIN Centre has helped 69 startups and MSMEs kickstart 72 chip design projects. These companies are developing everything from automotive ICs and power management chips to AI accelerators and security processors.

For many of them, ChipIN Centre has been launchpad offering not just tools, but also a support system including access to Multi-Project Wafer (MPW) runs and enablement of packaging, and post-silicon validation. This ecosystem allows them to focus on innovation while the Centre takes care of the rest.

One of the most remarkable things about ChipIN Centre is how it maintains global design standards while operating at a national scale. By aligning its services with international best practices, ChipIN Centre is helping Indian designers dream beyond borders. This blend of global competence and local relevance is what makes ChipIN Centre truly unique.

Modern chip design requires heavy computation, especially during simulation and verification. To meet this demand, ChipIN Centre provides access to Param Utkarsh Supercomputing Facility, one of India's powerful HPC platforms. Institutes and startups using ChipIN infrastructure can run intensive workloads without having to invest in their own hardware. Design teams can now reduce design time, accelerate verification, and improve product quality.

ChipIN centre – CATALYSING INDIA'S CHIP DESIGN REVOLUTION

The Centre is not just about tools and infrastructure. It also plays a major role in training, mentoring, and handholding. From conducting webinars and workshops to enabling expert technical support, the Centre ensures that users at all levels are guided through their chip design journey.

Many faculty members who had limited exposure to chip design are now confidently guiding student projects. Startups that were once struggling with tool licenses are now presenting at global conferences. Institutions that had never participated in chip prototyping are now working on ASIC tape-outs.

ChipIN Centre is not just enabling design—it is building confidence. Colleges are introducing elective courses based on EDA tools hosted at ChipIN Centre. Hackathons, grand challenges, and collaborative research are thriving. ChipIN Centre is playing a silent yet powerful role in all of this, providing the backbone for a self-sustaining ecosystem.

Conclusion – A Strong Foundation for India's Chip Design Journey

ChipIN Centre is not just a facility—it is a catalyst in shaping India's semiconductor future. By bringing together essential infrastructure, design tools, compute resources, and expert guidance, it has created a strong and inclusive foundation for students, researchers, startups, and MSMEs to confidently progress from ideas to actual silicon chips. It has simplified access to advanced technology, encouraged innovation, and built bridges between academia and industry.

India's semiconductor journey is still at an early but promising stage. The momentum created through initiatives like ChipIN is already visible—more institutions are participating in MPW shuttles, more students are experiencing real-world chip design, and more startups are stepping into the design ecosystem. This wave of activity is building local capability and reducing dependence on imported solutions. A new generation of engineers is being trained on industry-relevant platforms, and innovation is being nurtured across the country.

The path forward is both exciting and achievable. The focus will be on scaling up successful models—expanding MPW shuttles, enhancing access to compute infrastructure, supporting the development and reuse of IP cores, etc. Strengthening collaboration with domestic and global foundries, packaging units, and test labs will ensure end-to-end support for product realization. Continued emphasis will also be placed on nurturing commercial success—helping designs move beyond prototypes to reach real-world deployment.

As India moves ahead in establishing itself as a key player in the global semiconductor space, ChipIN Centre will remain a vital enabler. It will support creativity, nurture technical excellence, and drive innovation across all levels of the ecosystem. Students, researchers, startups, and MSMEs will continue to find the support they need to innovate and grow. The journey has begun, and with every chip designed, every prototype tested, and every startup supported, a stronger and more self-reliant India is steadily taking shape.

INDIGENOUS HPC PROCESSORS AND AI/ML HARDWARE ACCELERATORS

Shri Anoop Kumar
Scientist F
C-DAC Hyderabad

The development of indigenous High-Performance-Computing (HPC) Processors and AI/ML hardware accelerators is gaining significant momentum with partnerships, driven by the growing need for data sovereignty, security, and technological self-reliance. Countries are actively investing in local processor ecosystems to reduce dependency on foreign semiconductor supply chains and to build specialized hardware that caters to emerging AI/ML workloads.

Combining indigenous HPC Processor development with specialized AI accelerators presents several strategic advantages with step towards technological independence.

Data Sovereignty: Ensures that sensitive data remains within national borders, enhancing security.

Customization: Indigenous AI accelerators can be optimized for regional AI applications like agriculture, healthcare, and natural language processing in native languages.

Cost Efficiency: Locally designed HPC Processors and AI accelerators can reduce licensing costs and dependencies on foreign chipmakers.

Strategic investment in talent development, research partnerships, and manufacturing capabilities will be crucial for success in this frontier.

Considering the above aspects, as part of Govt. of India's National Supercomputing Mission (NSM), C-DAC is working towards development of indigenous HPC Processor (AUM) and AI/ML Accelerator.

HPC PROCESSOR AUM

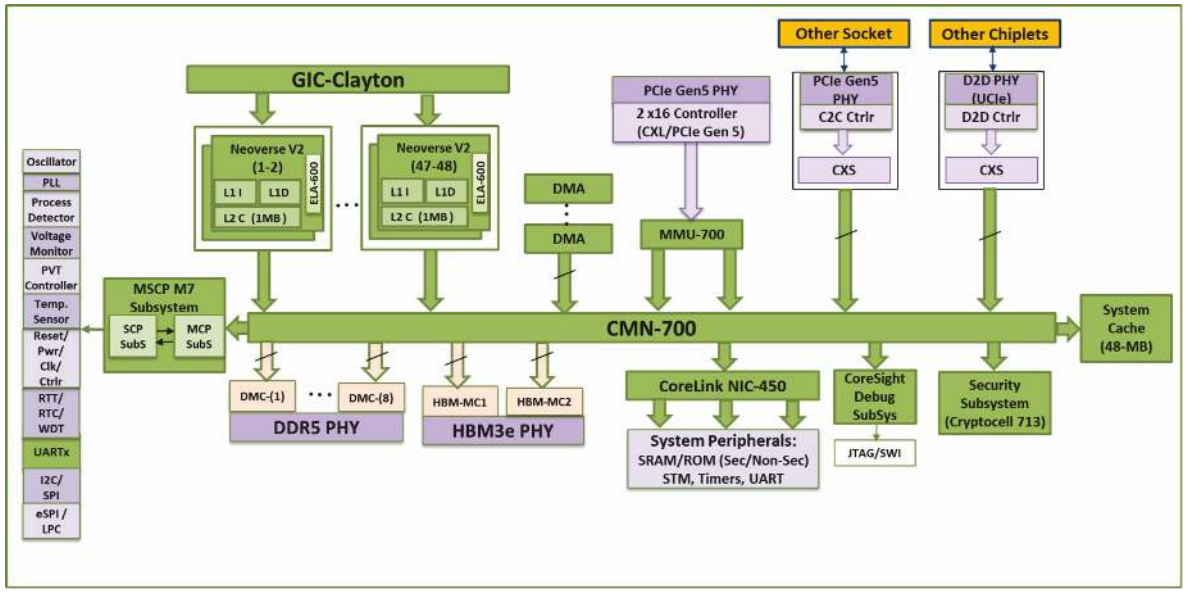
Introduction

The global race for technological sovereignty has placed High-Performance-Computing (HPC) at the forefront of national strategic priorities. Recognizing this, India's National Supercomputing Mission (NSM) has embarked on a transformative journey to achieve self-reliance in HPC. Keeping an alignment with the "Aatmanirbhar Bharat" initiative of Government of India, for complete indigenization of HPC System development, as part of National Supercomputing Mission, C-DAC is developing an indigenous HPC-AI Processor SoC (AUM) and Dual Socket Server. These indigenous developments will enable future Exa-Scale HPC System development.

AUM Processor is having HPC and AI capabilities and is targeted for HPC, AI and Cloud markets. Major features include - 5nm Technology Node, Chiplet based architecture, 2-Chiplets, 96-Cores and upto 128-GB HBM3e memory in a socket.

Key Features of AUM Processor

- **High-Performance Architecture**
  - 96-core power-efficient ARM-based design
  - HBM3e for high bandwidth memory accesses (useful in AI applications)
  - DDR5 for high density memory accesses
  - PCIe Gen5 / CXL for interfacing accelerators like GPUs



48-Cores Chiplet

HPC PROCESSOR AUM

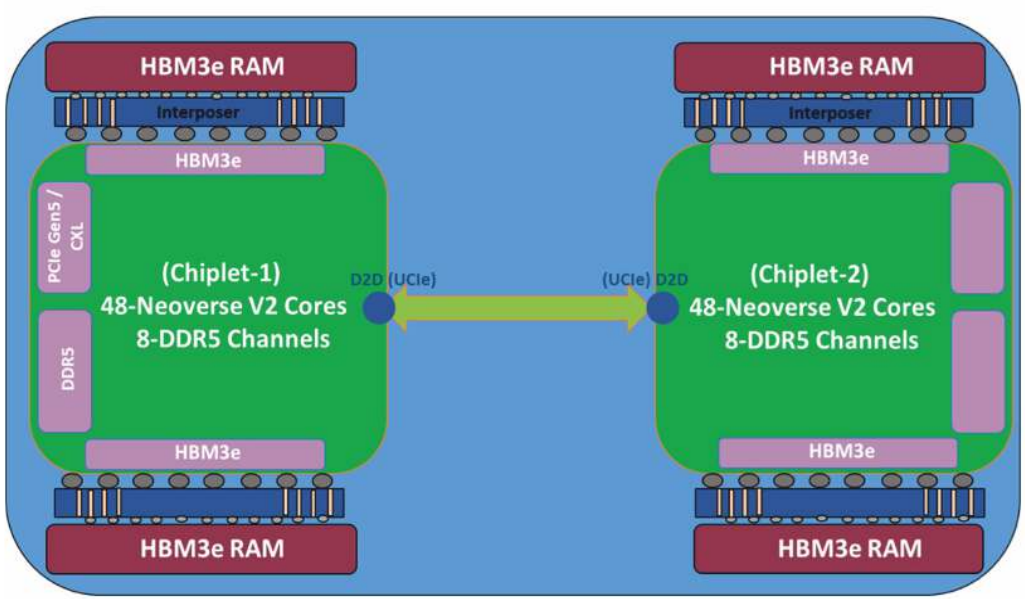
- **Chiplet-Based architecture**
  - Die-to-Die (D2D) Interconnects for modular scalability
  - 2.5D Advanced Packaging, hosting HBM directly on the SoC, improving bandwidth and power efficiency.

- **Manufacturing & Process Technology**
  - Fabricated on TSMC's 5nm process node, ensuring high performance and power efficiency.

- **Industry Collaboration & Roadmap**
  - Development in partnership with Indian Semiconductor Industry

- **Development of Indigenous Software Stack**
  - Creating a fully integrated software ecosystem

- **Availability**
  - Tested samples of AUM Processor are expected by Q1 2027
  - Dual Socket Compute node based on AUM Processor is expected by Q3 2027



AUM Processor – 96 Cores

Conclusion

The AUM Processor under NSM represents a transformative leap towards India's technological self-reliance in High-Performance-Computing.

With the successful realization of the AUM initiative, India is on track to emerge as a global leader in High-Performance-Computing, AI acceleration, and Semiconductor innovation—cementing its place in the technological landscape of the future.

INDIGENOUS AI ACCELERATOR

Large language models (LLMs) like GPT-4, Deepseek, Perplexity had taken the AI solutions to a new level by generating response in natural languages, code of a program etc. Investing in the R&D of AI Accelerators is a strategic move for companies, governments, and institutions due to the transformative impact of artificial intelligence (AI) across industries. As AI models grow in complexity and size, general-purpose processors (like CPUs) struggle to keep up. Focused R&D in AI accelerator design can unlock significant advantages.

Memory wall & opportunity for custom hw designs:
In the last decade compute power delivered through VLSI / semiconductor chips has increased by 10x whereas the memory access capacity is only inceased by 4x. CPU computes floating point operations (FLOPs) much faster than memory bandwidth and capacity, creating the memory wall where the memory system can no longer feed the compute efficiently. The disproportionate increase in compute-memory ratio created opportunity to go for custom design to meet training & inference needs in AI-ML domain.

Light weight PEs (Processing Elements) can bring down the power and area costs while increasing the computation speed up with data optimization flow. This customized hardware design leading to AI-ML accelerators in achieving the accelerated operations with lesser power.

Indigenous AI/ML Hardware Accelerator:
With the overall objective to design and develop indigenous AI Accelerator chip for the future needs of exa-scale computing that supports both training and inference under HW-SW co-development methodology. Since this is fairly involved and complex. It is being pursued in collaboration with industry.

Feature set:
The Feature set targeted for the AI-ML accelerator is as below:

- AI Accelerator for both training and inference work loads
- On-chip scratch memory & matrix buffers
- Systolic array-based parallel matrix multiplication
- Accelerating through activation functions and Pooling
- Supported computation formats INT8, INT16, INT32, FP16, FP32
- Data fetch & computation parallelization through DMA
- Acceleration through Multi clusters
- Handling sparsity through zero skipping algorithms

Design:
Core of the accelerator is Systolic Array. it is designed to perform matrix operations of maximum size 64x64 in one go. Once Input matrix & Weight matrix are loaded into the buffer, it performs the chosen operation like multiplications and the resultant matrix is moved into the accumulator block. Activation and pooling operations can follow once the basic operation is performed. This can happen in parallel while DMA is fetching the data for the subsequence operations.

Core of the accelerator is **Compute** IP with 4 systolic array (SA) units of size 64x64. it is designed to perform 16K MAC operations in one go.

INDIGENOUS AI ACCELERATOR

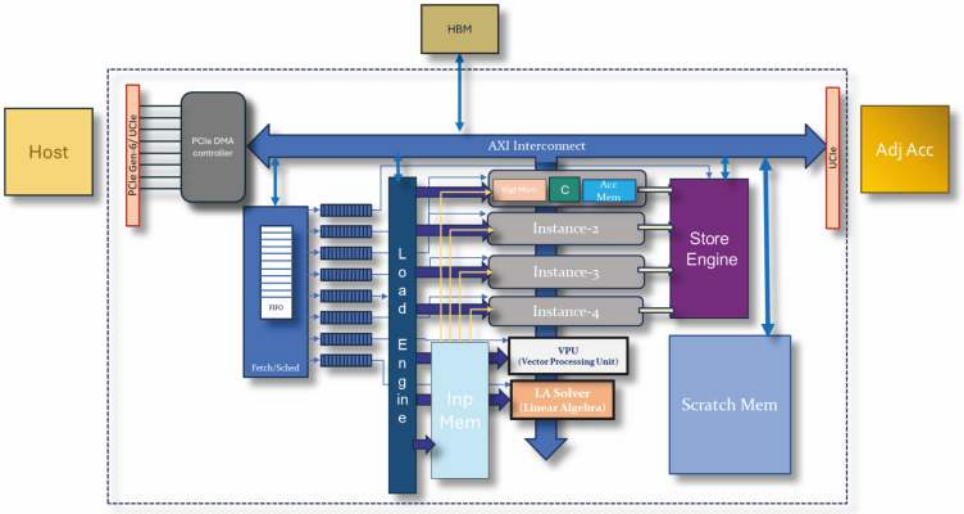
Data types:
Data types play a major role in determining accuracy of the outcome by the AI model. Typically training workloads use FP32 (single precision floating point) data type for the inputs and weights for better accuracy. Once the model is trained the trained wight data can be quantised to INT8 for inference without losing the outcome of the application. Industry has come up BF16 which giving the same value range as FP32 and decimal range as FP16 for better performance. The newer data types, BF16, FP8, INT4 which are emerging are being considered for the futuristic needs.

Impact:
We are very certain that the implementation and commissioning the indigenous AI Accelerator will certainly make a positive impact in the following ways.

Economic and Strategic Importance: AI is a key driver of economic growth and innovation across sectors like healthcare, finance, manufacturing, and transportation. Countries and companies investing in AI accelerator R&D can secure a leadership position in the global AI race, reducing dependence on foreign technology.

National Security and Sovereignty: AI accelerators are critical for defense, cybersecurity, and intelligence applications. Countries investing in domestic AI hardware reduce reliance on foreign suppliers, enhancing national security and technological sovereignty.

Environmental Impact: AI accelerators are designed to be more energy-efficient, reducing the carbon footprint of AI training and inference. This aligns with global sustainability goals and



IDEAS TO ACTION

NEW MEITY PROJECTS

IDEAS TO ACTION

1

Name of Project:

Deep Dive Underwater Drone -1K

CI: Shri Vishnu S, Scientist -E, C-DAC Thiruvananthapuram

Co-CI: Shri Harikrishnan C S, Scientist -E, C-DAC Thiruvananthapuram

Collaborators: IIT Bombay

Brief Description:

Design development and field evaluation of deep water Work Class ROV (Remotely Operated Vessel) with 1000m depth rating. The project is a part of Pushpak National Mission on drone technology with IIT Bombay as the nodal agency.

NEW MEITY PROJECTS

IDEAS TO ACTION

2

Name of Project:

Enabling Secure Boot in RISC-V Processors Using Post-Quantum Secure Schemes

Co-CI: Ms. Sajna V P, Scientist -E, C-DAC Thiruvananthapuram

Collaborators: Society for Electronic Transactions and Security (SETS), Chennai

Brief Description:

The primary objective of this project is to demonstrate secure boot functionality using classical and post-quantum cryptographic schemes by integrating with the indigenously developed VEGA processor along with a mechanism of on-chip generation of keys.

NEW MEITY PROJECTS

IDEAS TO ACTION

3

Name of Project:

Web Portal for STQC Lab Automation

CI: Shri Gour Mohan, Scientist E, C-DAC Noida

Brief Description:

The STQC Web Application is designed to facilitate the digitization and automation of laboratory processes. It will serve multiple stakeholders, including STQC HQ, Certification Officers, Regional Managers, Lab Administrators, Customers, and others. The system will streamline certification processes, testing, calibration, payments, and inventory management. Additionally, it will support role-based access control, authentication mechanisms, complaint management, and comprehensive reporting.

NEW R&D PROJECTS
(EXTERNAL FUNDING)

IDEAS TO ACTION

4



Name of Project:

Administrative Education and Training Portal (AETP)

CI: Shri Ritesh R. Dhote, Scientist E, C-DAC Patna

Co-CI: Shri Amarjeet Sharma, Scientist C, C-DAC Patna
Shri Santosh Kumar, Scientist C, C-DAC Patna

Funding Agency: Administrative Training Institute, Department of Atomic Energy

Brief Description:

The Administrative Education and Training Portal (AETP) is a proposed digital platform aimed at modernizing and streamlining administrative training programs under the Department of Atomic Energy (DAE). This application is currently in the development phase and will provide a centralized, user-friendly, and efficient system for managing training programs, course nominations, approvals, and trainee records.

NEW R&D PROJECTS
(EXTERNAL FUNDING)

IDEAS TO ACTION

5

Name of Project:

Digital Archival and Retrieval System for Historical Documents at IIM Calcutta

CI: Shri Niladri Sekhar Saha, Scientist E, C-DAC, Kolkata

Funding Agency: Indian Institute of Management (IIM), Calcutta

Brief Description:

This project aims to develop a comprehensive digital archival and retrieval system for the historical documents preserved at the Indian Institute of Management Calcutta (IIM Calcutta). The initiative will focus on the digital preservation, and intelligent retrieval of rare and valuable documents, including administrative records, research publications, correspondence, and institutional reports that reflect the rich academic and administrative legacy of the institute.

NEW R&D PROJECTS
(EXTERNAL FUNDING)

IDEAS TO ACTION

6

Name of Project:

Study of Learning Record Store Interoperability Augmented by Blockchain

CI: Shri N Satyanarayana, Scientist E, C-DAC Hyderabad

Funding Agency: Bureau of Indian Standards

Brief Description:

This study aims to enhance the tracking of students' learning capabilities by moving beyond traditional credit-based evaluation to a more granular approach that captures their understanding of subject concepts. Such a data will give us an accurate information about the student's strengths and acquired skill sets. Standardization efforts, particularly through Experience API (xAPI), enable digitalization of this data, allowing institutions to assess students' strengths accurately. The scope of this proposal is to define a common vocabulary for Learning Record Store (LRS) statements based on classification of cognitive skills (e.g., Bloom's Taxonomy) and store such information in all LMS/LRS instances managed by different educational institutions in which the student has enrolled to pursue his/her study in their academic journey. Blockchain interoperability is being explored as a potential technology backend to accomplish the above-mentioned task that facilitates maintaining a tamper-proof and unique state of information.

PROGRESS PULSE:

A PERFORMANCE DASHBOARD

IPR PORTFOLIO

To create awareness and increase the Intellectual Property Rights (IPR) footprint across C-DAC, the Corporate IPR Cell has been established. Details of the IPR activities of C-DAC during this quarter are as below:

	IPR portfolio of C-DAC (Year 2013 to March 2025)				Quarterly IPR portfolio of C-DAC (January 2025- March 2025)			
	Patents	Copyrights	Trademarks	Design	Patents	Copyrights	Trademarks	Design
Applied/Filed (Pending)	64	16	34	2	6	6	5	1
Granted/Registered	110	186	23	4	3	7	0	0
Total	174	202	57	6	9	13	5	1

MAJOR PROJECT PERFORMANCE/ STATISTICS

DESIGN LINKED INCENTIVE SCHEME (DLI)

The Design Linked Incentive (DLI) Scheme aims to provide financial incentives as well as design infrastructure support across various stages of development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design with an aim to achieving significant indigenization in semiconductor and electronic products and IPs deployed in the country, thereby facilitating import substitution and value addition in electronics sector in the next 5 years. As per the approval accorded by Cabinet, DLI Scheme is being implemented by C-DAC.

The Design Linked Incentive (DLI) Scheme shall offer financial incentives as well as design infrastructure support across various stages of development and deployment of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design over a period of 5 years.

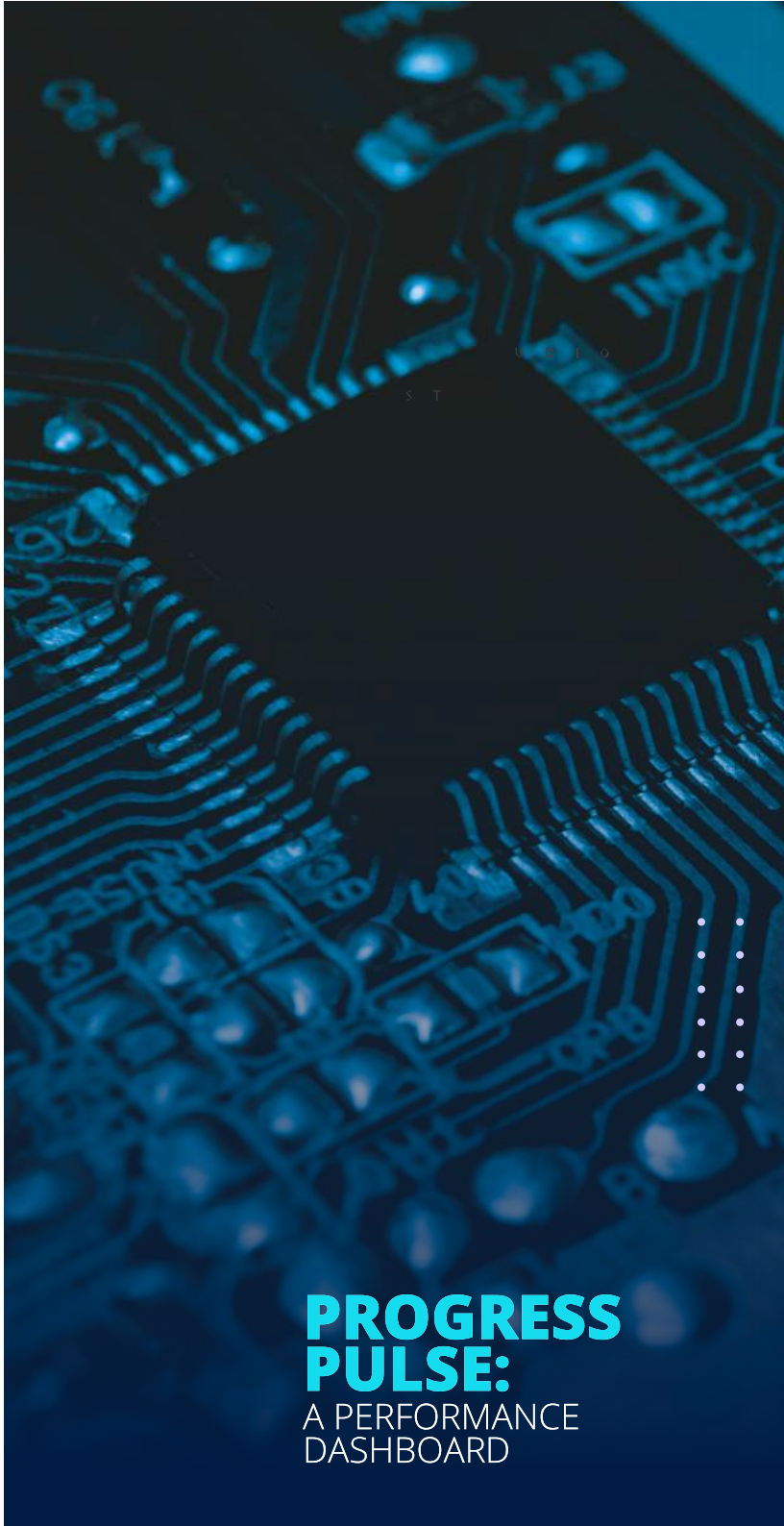
Application Status		
DLI Applications	Proposals	
	Product Design linked Incentive/ Design linked Incentive	EDA Tools Access Request
Proposals Received	115	76
Evaluation Ongoing	54	01
Proposals Approved	17	70
Proposals Rejected	44	05

PROGRESS PULSE:
A PERFORMANCE DASHBOARD

MAJOR PROJECT PERFORMANCE/ STATISTICS

DETAILS OF APPROVED APPLICANTS FOR FINANCIAL SUPPORT UNDER DLI SCHEME

Approved applicants for Fiscal Support under DLI Scheme (PDLI)			
No.	**Applicants**	**Approved incentives under the DLI Scheme (Rs. In Lakhs)**	**Funds disbursed (Rs. In Lakhs)**
1.	Saankhya Labs Pvt Ltd	1138.3	216.42
2.	Aheesa Digital Innovations Private Limited	1500	886.08
3.	Fermionic Design Private Limited	413.91	248.74
4.	Vervesemi Microelectronics Pvt Ltd	1353	249.35
5.	Morphing Machines Pvt Ltd	1024.4	22.08
6.	Sensesemi Technologies Pvt. Ltd.	1500	101.02
7.	Aryabhata Circuits and Research Labs Private Limited	1500.02	0
8.	MINDGROVE TECHNOLOGIES PRIVATE LIMITED	1500	198.73
9.	WISIG NETWORKS PRIVATE LIMITED	1267.79	85
10.	Netrasemi Private Limited	1500	669.35
11.	InCore Semiconductors Private Limited	823.5	58.54
12.	GREEN PMU SEMI PRIVATE LIMITED	484.01	91.37
13.	Calligo Technologies Private Limited	1475.5	264.67
14.	BigEndian Semiconductors Private Limited	1500	218.26
15.	C2i Semiconductors Private Limited	1500	38.21
16.	MOSCHIP TECHNOLOGIES LIMITED	1500	454.57
17.	DV2JS Innovation LLP	341.5	103.42
	Total	**20321.93**	**3905.81**

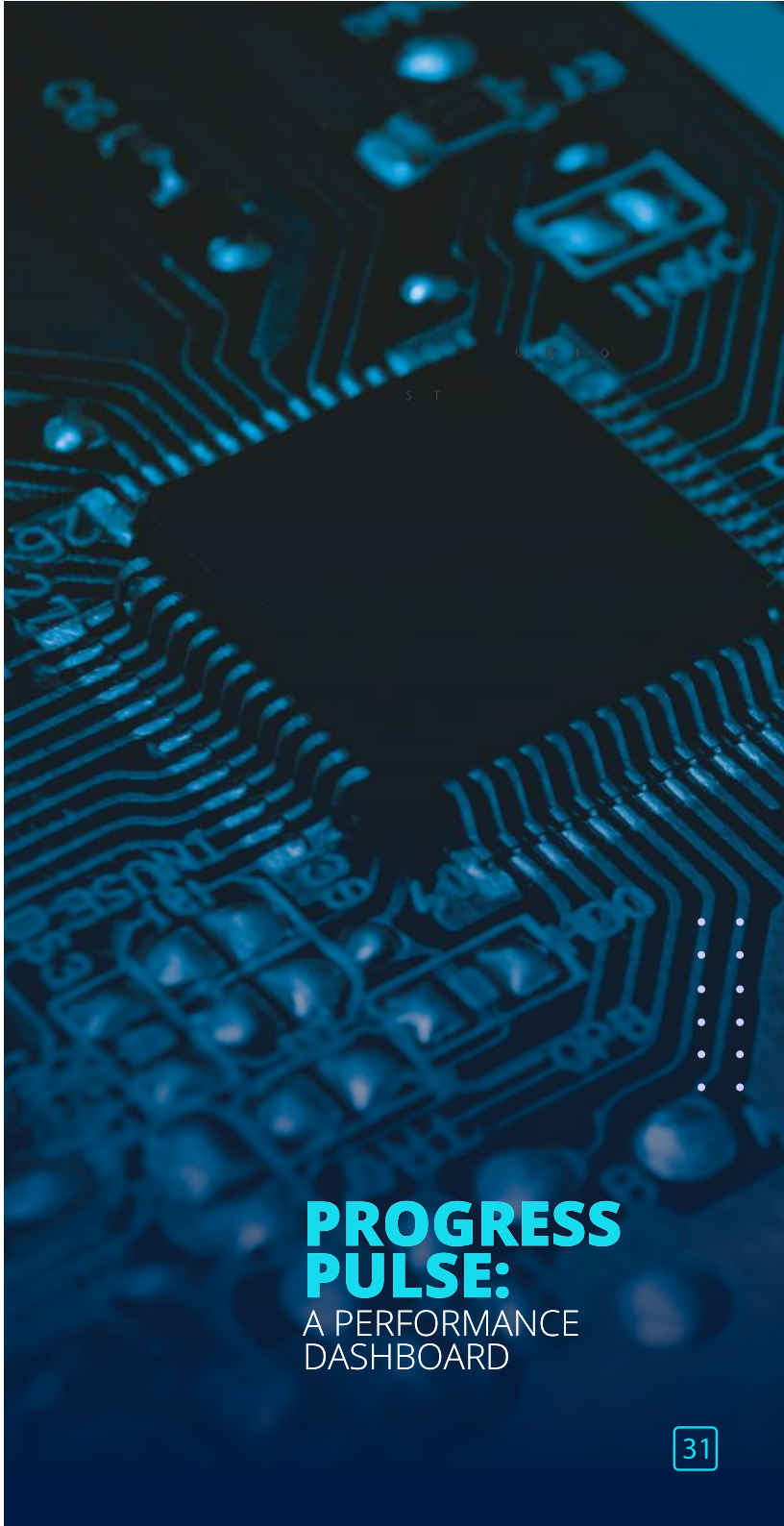


MAJOR PROJECT PERFORMANCE/ STATISTICS

DETAILS OF APPROVED APPLICANTS FOR FINANCIAL SUPPORT UNDER DLI SCHEME

Achievements – DLI Funded Applicants	
Applicant Name	**Achievements and Outcomes**
Fermionic Design Private Limited	• Successfully taped out X-band Beamformer 8-12GHz 4T4R IC. • Successfully demonstrated the silicon performance to customers. • Raised VC funding of Rs 50 Cr
Netrasemi Pvt Ltd	• Raised Investor funding of Rs 18 Cr
Green PMU Semi Pvt Ltd	• A total of 11 tape-outs have been successfully completed • Raised funding of Rs 6.5 Lacs from WxBunka Foundation, Japan
Morphing Machines Pvt Ltd	• Raised VC funding of Rs 23.80 Cr
Calligo Tech. Pvt Ltd	• Received the 1st version of fabricated design in March' 2024. • A total of 100 SoC have been fabricated. • Raised Investor funding of Rs 6.50 Cr
Sensemi Technologies Pvt Ltd	• Architecture and Specifications finalised with the potential customer • Raised VC funding of Rs 80 Lacs.
Mindgrove Technologies Private Limited	• Raised VC funding of 67.50 Cr
Incore Semiconductors Pvt ltd	• Raised VC funding of Rs. 24.6 Cr
BigEndian Semiconductors	• Raised VC funding of Rs. 22 Cr
C2i Semiconductors	• Raised VC funding of Rs. 18.25 Cr

Outcomes – DLI Scheme	
Manpower Generated	807
IP Cores Generated	39
SoC Fabricated	100



MAJOR PROJECT PERFORMANCE/ STATISTICS

DESIGN AND DEVELOPMENT OF A UNIFIED BLOCKCHAIN FRAMEWORK FOR OFFERING NATIONAL BLOCKCHAIN SERVICE AND CREATION OF ECOSYSTEM

It is an initiative to make India ready for large scale adoption of Blockchain technology and enable trust for applications in the domain of e-Governance. It focuses on enabling Blockchain-as-a-Service and addresses the research challenges across various layers of the Blockchain stack. The stack consists of several components such as a dashboard for automated network setup, generic smart contract layer, authentication and authorization functions and a set of Open APIs for accessing the Blockchain application. It includes security vulnerability assessment test suites for auditing smart contracts and Interoperability support between Hyperledger Fabric & Sawtooth Blockchain platforms.

Overall Project Status:

- Blockchain-as-a-Service (BaaS) enabled permissioned Blockchain based NBF
- Technology Stack is developed
  - Three Blockchain Platforms are supported and is extensible
  - Security Audit and Assessment Tools, Guidelines & Best Practices is complete
- NBFLite, a sandbox platform for rapid prototyping of applications, carrying out research and capacity building is developed. This is being used by Industry / Startup: 7, Govt Dept: 5 and Academia: 6)
- 10+ Blockchain based Applications are developed/ongoing in collaboration with different ministries / departments
- Security, Privacy & Performance Enhancement, and Interoperability Research efforts are made
- BaaS enabled NBF Technology Stack is hosted on geographically distributed infrastructure at NIC Data centres (Bhubaneswar, Pune, Hyderabad)
- Organized Workshops / User Meets with Government Departments / Skilling Courses
- Patents (5) and Technical Publications (51)
- Contributed to Standards
- Proposal was submitted for Grand Challenge and recommended by working group for onboarding applications of startups/ industry
- NBF Portal (https://blockchain.meity.gov.in)

PROGRESS PULSE:
A PERFORMANCE DASHBOARD

MAJOR PROJECT PERFORMANCE/ STATISTICS

MOBILE SEVA (MOBILE SERVICE DELIVERY GATEWAY)/ MOBILE SEVA APPSTORE

Mobile Seva platform is an innovative initiative aimed at mainstreaming mobile governance in the country. It provides an integrated whole-of-government platform for all Government departments and agencies in the country for delivery of public services to citizens and businesses over mobile devices using SMS, IVRS, CBS, LBS, apps. It is a centrally hosted cloud-based mobile enablement platform, which allows the departments to expeditiously start offering their services through mobile devices anywhere in India, without having to invest heavily in creating their separate mobile platforms. Over 5014 accounts of government departments and agencies with over 6548 cr+ transactions are integrated with Mobile Seva platform.

Mobile Seva platform		
	April 2012 to March 2025	**January 2025-March 2025**
Accounts of Dept/Agencies integrated	5080	66
No of Push SMS Transaction	**6548 Cr**	**172 Cr**

PROGRESS PULSE:
A PERFORMANCE DASHBOARD

MAJOR PROJECT PERFORMANCE/ STATISTICS

e-Hastakshar / e-Sign

As a flagship initiative within the Government's Digital India program, C-DAC has introduced e-Hastakshar, a cutting-edge eSign service that allows citizens to digitally sign documents online in real-time, providing a legally acceptable form and convenient alternative to physical signatures. Over the past year, C-DAC integrated this service with various departments, ministries, and agencies at the Central and State Government levels, as well as Union Territories. C-DAC utilizes service of Unique Identification Authority of India (UIDAI) for on-line authentication and Aadhaar eKYC service. e-Hastakshar service supports Online Aadhaar Authentication Modes - One-time password (OTP), TOTP, Fingerprint, IRIS, Face (Mobile Apps only) based modes of authentication for leveraging eKYC service of UIDAI.

As of March 2025, C-DAC has issued over 26.27 crore e-Signs. More than 270 government agencies are utilizing C-DAC's eSign service at the production level. Recently onboarded agencies include Department of IT Manipur, Inspector General of Registration Assam, Bihar State Electronics Development Corporation Limited and Tea Board India. In addition, key agencies such as the National Informatics Centre, Employees' Provident Fund Organisation, Keral State IT Mission, Tamil Nadu e-Governance Agency (TNeGA) and the Centre for e-Governance, Karnataka, are leveraging eSign at the production level.

eSigns offered by C-DAC	
July 2016 to Mrach 2025	**January-March 2025**
26.27 Crs.	5.06 Crs.

PROGRESS PULSE:
A PERFORMANCE DASHBOARD

MAJOR PROJECT PERFORMANCE/ STATISTICS

eSanjeevani

eSanjeevani, the flagship telemedicine platform of the Ministry of Health & Family Welfare, Government of India, stands as the world's largest telemedicine implementation in primary care. Harnessing the power of digital technology, the platform has redefined how healthcare reaches underserved populations, especially in rural and remote areas, by enabling easy access to quality medical consultations from anywhere.

Currently, eSanjeevani operates through an expansive network comprising over 1.31 lakh Ayushman Arogya Mandirs (AAMs) as spokes and more than 17,000 hubs, supported by a dedicated pool of over 2.3 lakh doctors, specialists, and healthcare workers across all States and Union Territories. This nationwide telemedicine ecosystem plays a pivotal role in delivering timely medical care while easing the strain on conventional healthcare infrastructure. With an impressive daily average of 4.5 lakh consultations—peaking at 6.3 lakh—and the infrastructure to support up to 10 lakh consultations per day, eSanjeevani exemplifies scalability and innovation in digital health. It continues to advance India's vision of equitable, accessible, and tech-enabled healthcare for all.

eSanjeevani Usage Report				
	November 2019 to March 2025		January 2025 to March 2025	
	Total Tele-Consultations	Registered Doctors	Total Tele-Consultations	Registered Doctors
eSanjeevaniAB-HWC	34,89,60,829	62,653	3,03,35,728	1,902
eSanjeevaniOPD	1,23,38,348	12,739	2,38,465	201
eSanjeevani	**36,12,99,177**	**75,392**	**3,05,74,193**	**2,103**

MAJOR PROJECT PERFORMANCE/ STATISTICS

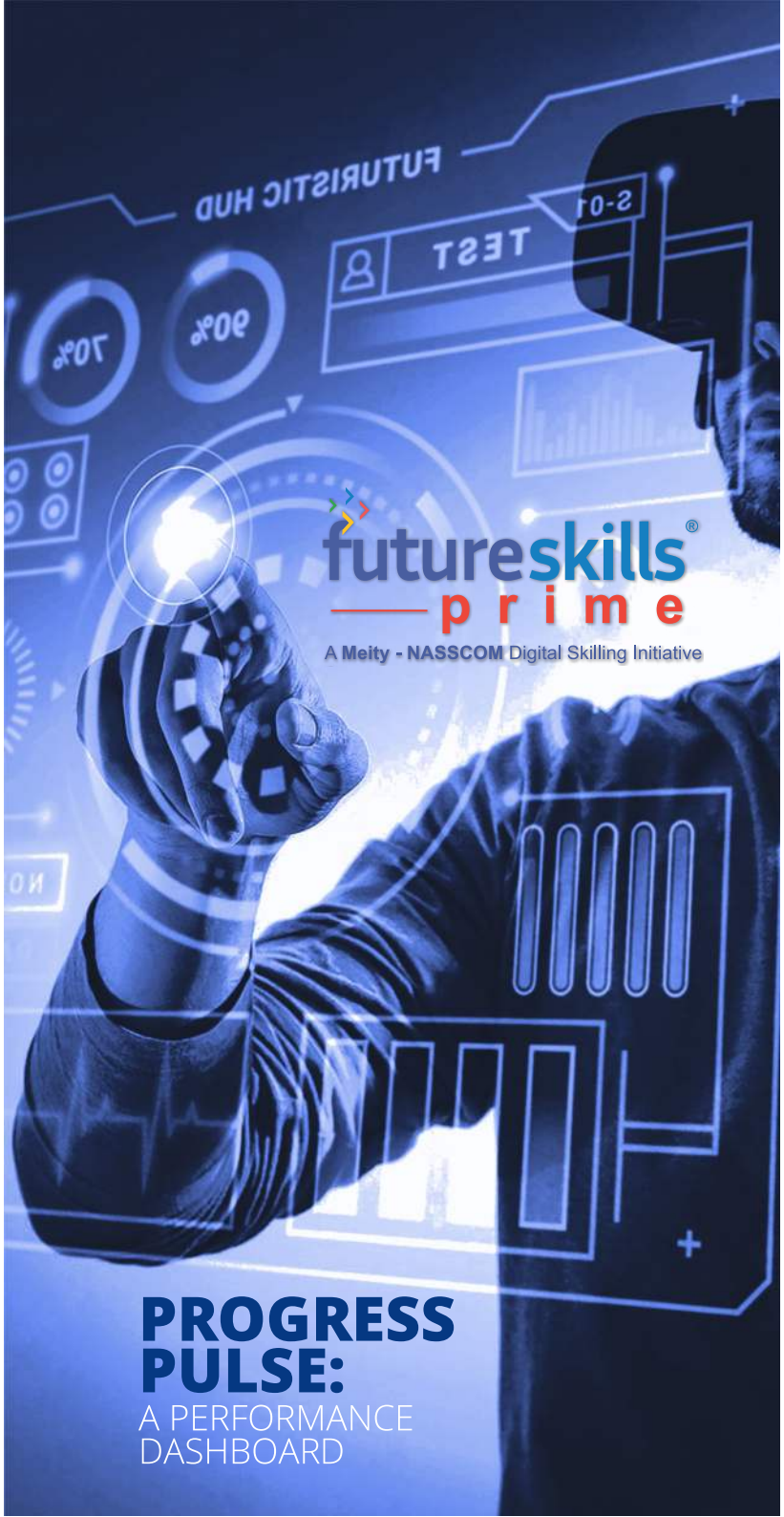
FUTURESKILLS PRIME (PROGRAMME FOR RE-SKILLING/UP-SKILLING OF IT MANPOWER FOR EMPLOYABILITY)

The Ministry of Electronics and Information Technology (MeitY) in association with NASSCOM has launched the FutureSkills PRIME (FSP) program, a pivotal initiative aimed at enhancing skills and knowledge in emerging technologies viz, Additive Manufacturing/3D Printing, Artificial Intelligence, Augmented/Virtual Reality, Big Data Analytics, Blockchain, Cloud Computing, Cyber Security, Internet of Things, Robotic Process Automation, Social & Mobile etc. The detail of the program is available in the https://futureskillsprime.in/ portal.

The FSP program provides reskilling/upskilling and experiential learning in disruptive technologies, through strategic partnerships with C-DAC/NIELIT Centers, Industries, Academia, Professional Bodies etc. FutureSkills PRIME activities involve Training Program in Emerging Technologies for Students & professionals, industry relevant Courses, to address the skill gap in niche technology areas. As part of phase 2, FSP aims to train around 10 Lakh Beneficiaries including career aspirants, employment seekers, non-IT employees in cross-pollinated digital roles, PSE employers, and IT employees across IT and non-IT sectors over the period of 3 Years through variety of Courses including (a) Bootcamp Courses (BCMP), (b) Government Officer Training- Basic (GOT-B), and (c) Government Officer Training – Advanced (GOT-A), (d) Deep Skilling, (e) Foundational (f) Experiential Learning.

As part of 1st Year of Phase 2 of FSP, overall, 22,756 Beneficiaries were from Bootcamp and GOT Programs conducted by C-DAC/NIELIT Ecosystem. Further, a total of 44 courses were developed under all technologies for Bootcamp, GOT-Basic and GOT-Advanced.

- PMU organized TechByte under the technology Cloud Computing by the C-DAC Chennai conducted on 25th Feb 2025.
- FSP Magazine has been published and launched on March 2025 showing the glimpse of the activities conducted by KIA, PMU for the year 2024.
- Over 42 webinars have been conducted, 80+ PSUs have undergone skilling, and 55+ universities have been engaged.

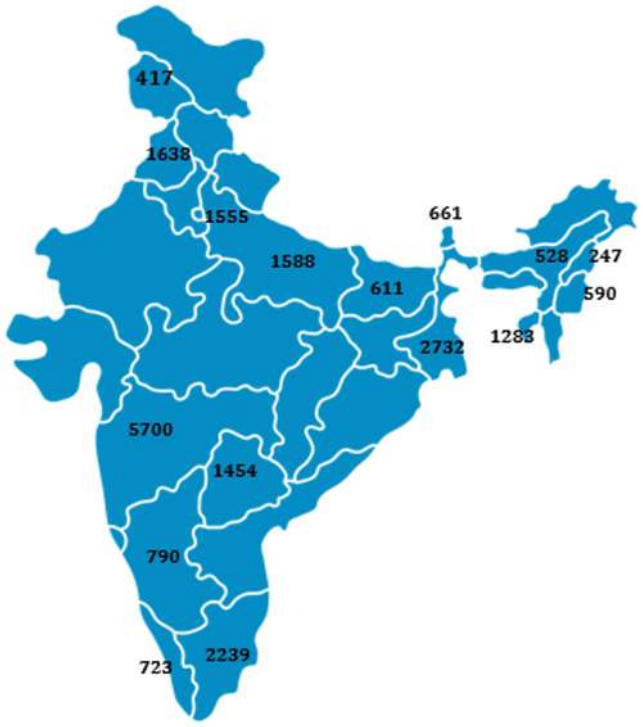


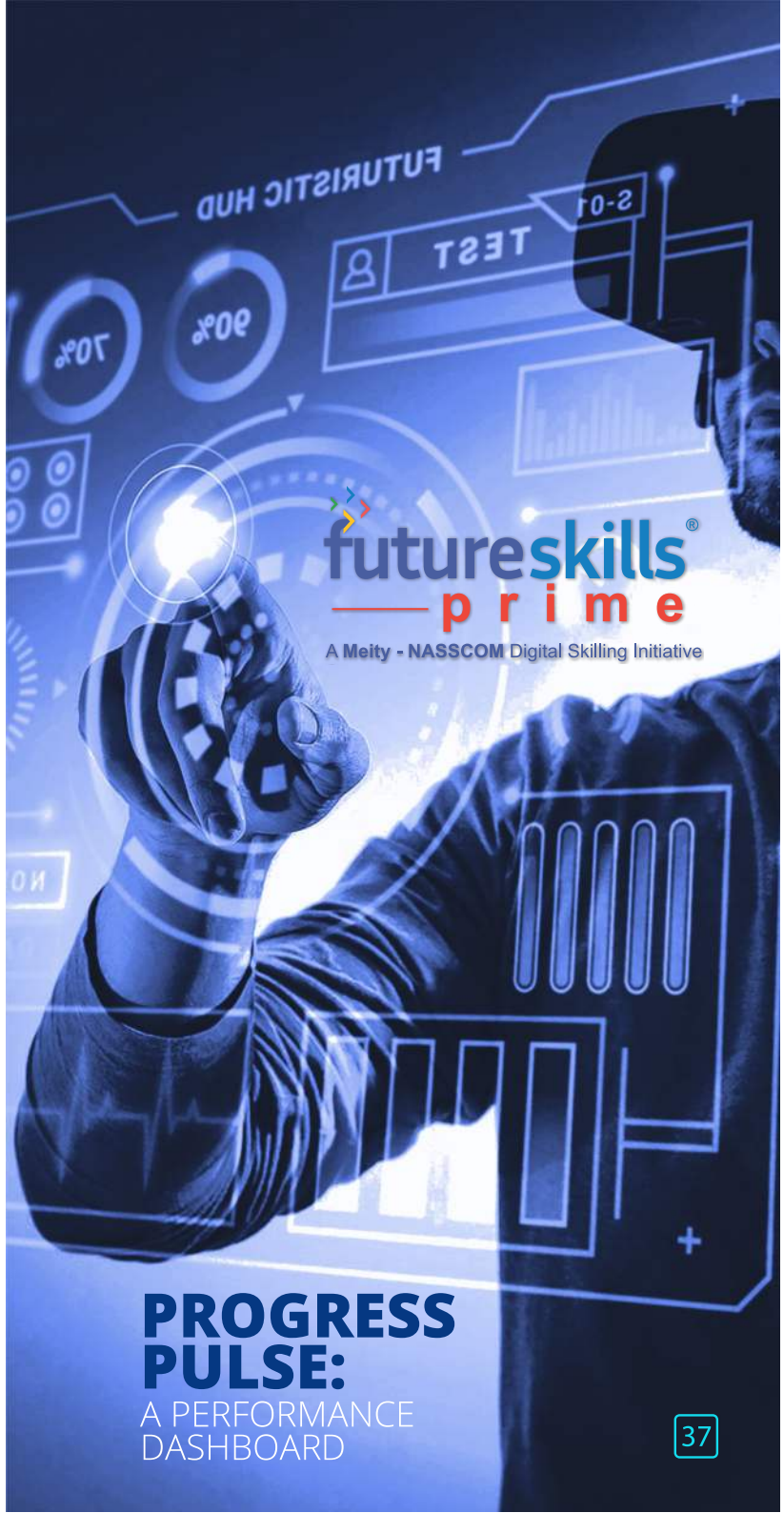
MAJOR PROJECT PERFORMANCE/ STATISTICS

FUTURESKILLS PRIME (PROGRAMME FOR RE-SKILLING/UP-SKILLING OF IT MANPOWER FOR EMPLOYABILITY)

Category/ Activity	Agency	1st April 2024- 31st Dec 2024	1st January 2025- 31st March 2025	Total Achievement (1st April 2024 – till date)
Government Training – Advanced	C-DAC/ NIELIT	1297	1668	2965
Government Training - Basic		1651	1536	3187
Bootcamp		7851	8753	16604
TOTAL LEARNERS		**10799**	**11957**	**22756**

States	No of Learner's certified under FSP
Telangana	1454
Assam	528
Bihar	611
Delhi	1555
Jammu & Kashmir	417
Karnataka	790
Kerala	723
Maharashtra	5700
Manipur	590
Nagaland	247
Punjab	1638
Sikkim	661
Tamil Nadu	2239
Tripura	1283
Uttar Pradesh	1588
West Bengal	2732





MAJOR PROJECT PERFORMANCE/ STATISTICS

eAUSHADHI DRUGS AND VACCINE DISTRIBUTION MANAGEMENT SYSTEM (DVDMS)

It is a web-based programme that manages the supply chain of pharmaceutical supplies such as medications, sutures, and surgical items needed by various Drug Warehouses/Drug Stores. The primary goal of DVDMS is to determine the pharmaceutical demands of the state drug programme and the MoHFW's national level programme for various drug warehouses/drug stores so that all necessary materials/drugs are always available to be given to patients/beneficiaries in the state without delay. This involves item classification/categorization, item codification, item quality control, and lastly issuing pharmaceuticals to patients, who are the end consumers in the chain.

eAushadhi (DVDMS) - Coverage across India alogwith Procurement and Issue Details for Drugs

Sl.no	Institutions	Jan 2023 to March 2025 (Amount in Crore)		January 2025 to March 2025 (Amount in Crore)	
		Procurement Value	Distribution Value	Procurement Value	Distribution Value
	A. States Implementation				
1	Andhra Pradesh	1993.44	1501.20	108.51	127.87
2	Assam	776.30	85.23	74.30	9.23
3	Bihar	1446.28	1399.6	157.89	162.83
4	Gujarat	1126.37	1131.09	152.14	103.32
5	Himachal Pradesh	251.09	232.70	33.09	27.90
6	Jharkhand	65.87	94.08	7.73	8.08
7	Madhya Pradesh	1432.49	1078.00	167.52	117.73
8	Maharashtra (PHD & DMER)	1005.96	1004.17	54.36	98.33
9	Punjab	7004.39	10111.58	378.53	1057.2
10	Rajasthan	5220.23	4259.57	682.96	470.52
11	Telangana	1117.68	1004.84	87.74	68.11
12	Uttarakhand	122.62	106.68	16.53	11.55
13	Uttar Pradesh	2129.99	375.86	216.22	268.68
	B. Union Teritories (UT) Implementation				
1	Jammu and Kashmir	722,67	579.6	46.15	111.78
2	Puducherry	232.35	710.77	52.7	19.39
3	Lakshadweep	549.11	1715.83	7	402.78
4	Chandigarh	6.00	8.32	3	1.68
	C. Centralized / National Implementations				
1	DGAFMS- Ministry of Defence (Army, Navy, Airforce and subsidaries)	1639.91	1034.61	503.29	209.785
2	Central Medical Services Society- MoHFW	5054.11	2814.09	560.52	445.34
3	Dept of Family Planning -MoHFW	1756.35	928.74	551.24	187.74
4	National Tuberclosis Elimination Programe-MoHFW	746.36	4966.1	7.21	218.71
5	Medical Stores Organization-MoHFW	433.07	576.74	48.99	52.70
	D. Other Implementations				
1	Directorate of Medical Insurance-Govt of Andhra Pradesh	61.33	9.12	1.09	0.7732
2	Directorate of Medical Insurance-Govt of Telangana	0.00	0	0	0

PROGRESS PULSE:
A PERFORMANCE DASHBOARD

MAJOR PROJECT PERFORMANCE/ STATISTICS

IPDMS 2.0, INTEGRATED PHARMACEUTICAL DATABASE MANAGEMENT SYSTEM 2.0

The Integrated Pharmaceutical Database Management System (IPDMS) 2.0 is a responsive, web-based application developed for the National Pharmaceutical Pricing Authority (NPPA). It streamlines and integrates the core functional processes necessary for monitoring and regulating the prices of drugs and medical devices.

Established on 29th August 1997 by a Government of India Resolution, the NPPA functions as an attached office under the Department of Pharmaceuticals (DoP), Ministry of Chemicals and Fertilizers. It is entrusted with the independent mandate of regulating drug pricing—including medical devices—to ensure their availability at affordable rates.

IPDMS 2.0, together with the Pharma Sahi Daam 2.0 mobile application (available on both Android and iOS platforms), provides users with real-time access to the prices of Scheduled and Non-Scheduled medicines at the point of purchase. Additionally, the Pharma Jan Samadhan platform offers a user-friendly interface for lodging and tracking four categories of complaints: overcharging, sale without prior approval, shortage or unavailability of medicines, and refusal to sell drugs. This complaint redressal mechanism is seamlessly integrated into both the Pharma Sahi Daam mobile app and the IPDMS 2.0 web portal.

The calculation of ceiling and retail prices of drugs, along with the associated overcharging workflows, has been automated and integrated into the IPDMS 2.0 application. These workflows are linked with 31 State Price Monitoring and Resource Units (PMRUs). Individuals can verify ceiling prices and register overcharging complaints directly through the mobile applications.

MAJOR PROJECT PERFORMANCE/ STATISTICS

IPDMS 2.0, INTEGRATED PHARMACEUTICAL DATABASE MANAGEMENT SYSTEM 2.0

Integration Pharmaceuticals Database Management System, IPDMS 2.0		
Activities done by Pharma/Medical Devices Companies & NPPA	till 31st Mar 25	Jan 2025 - Mar 2025
Total Companies (Drugs & Medical Devices) Registered in the IPDMS 2.0	1663 (1477- Drugs, 186 - Medical Devices)	61 (47 - Drugs, 14 - Medical Devices)
Number of Manufacturing Unit verified by the companies	8101	268
Number of Drugs verified by companies	57341	2160
Medical Devices Plant Registered	528	17
Medical Devices Registered	57208	1933
Quarterly Stock Collection	19961	2823
State Pricing Monitoring Resource Unit (PMRU) registered.	31	0
Form-I (Application for Price Fixation) Submitted	613	96
Form-II (Submission of Revised Prices) Submitted	14028	253
Form-III (Quarterly Return) Submitted	59147	7716
Form-IV (Discontinuation of Production) Submitted	135	4
Form-V (Price List) Submitted	80102	8133
Form – VI (Medical Devices) Submitted	52922	2288
Complaints Registered through Web and Mobile Apps	6300	498
Legal Cases Registered for Overcharging	761	33

PROGRESS PULSE:
A PERFORMANCE DASHBOARD

MAJOR PROJECT PERFORMANCE/ STATISTICS

CYBER GYAN

Cyber Gyan is a significant project entrusted to C-DAC Noida by the Ministry of Electronics and Information Technology (MeitY). Titled "Cyber Security Scenario-Based Self-Paced Learning Training Facility," the project is designed to equip SC, ST, and Economically Weaker Section (EWS) undergraduate and postgraduate students from government colleges across 8 North-Eastern states and 4 other states—Uttar Pradesh, Haryana, Gujarat, and Kerala—with critical cyber security skills.

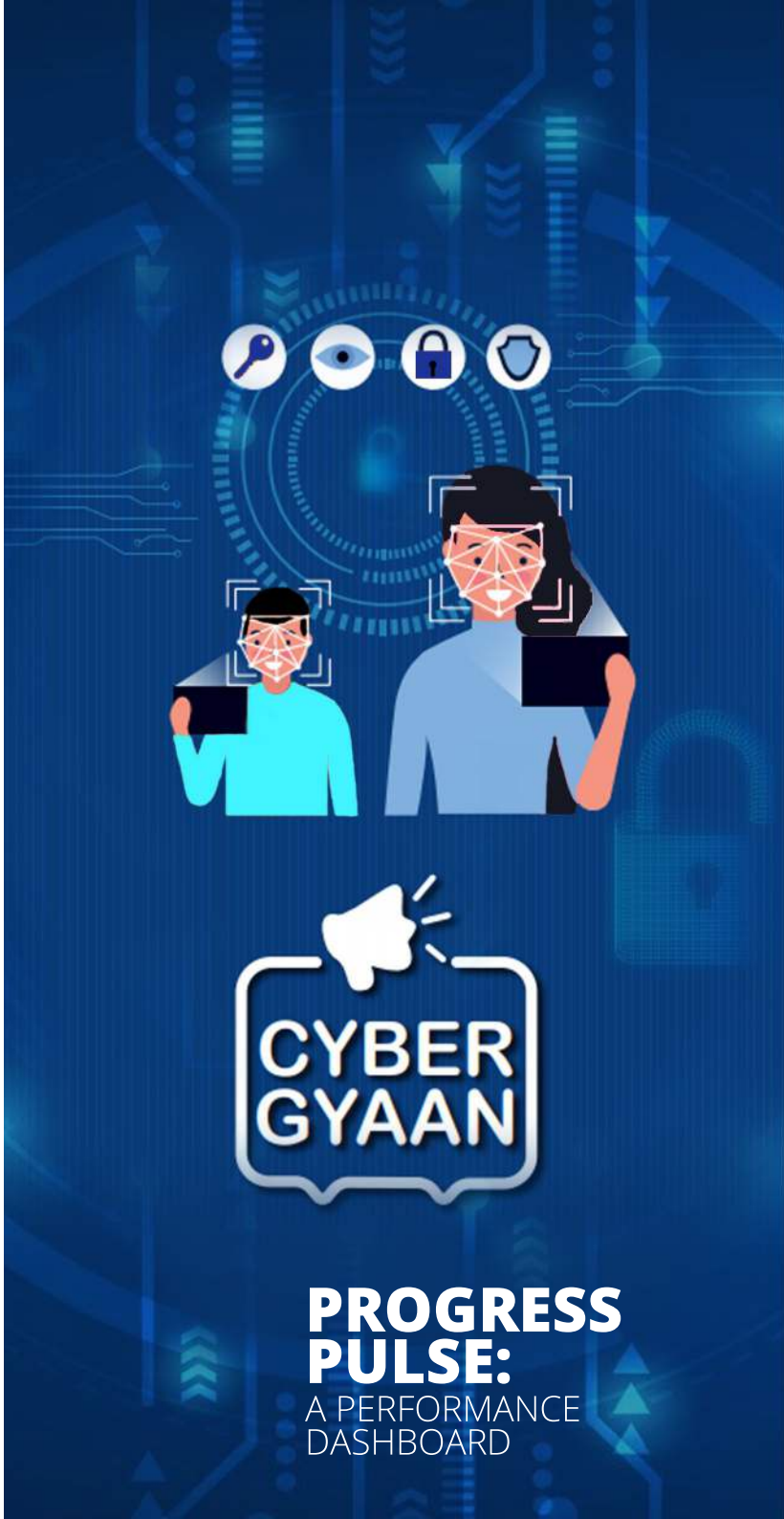
The initiative aims to develop skilled manpower in the rapidly evolving domain of cyber security, essential for protecting critical infrastructure from cyber threats and attacks. As a foundational step, over 530 faculty members from these 12 states have successfully completed Master Trainings under this program. These trainings were structured to empower faculty with hands-on knowledge and practical insights into various cyber security domains, enabling them to mentor and guide students effectively as local champions of cyber awareness and capacity building.

Now, this initiative has extended its opportunities nationwide, inviting students from government engineering colleges across India to participate—fostering a generation of cyber warriors capable of addressing modern digital challenges and contributing towards the creation of a cyber-resilient nation.

MAJOR PROJECT PERFORMANCE/ STATISTICS

CYBER GYAN

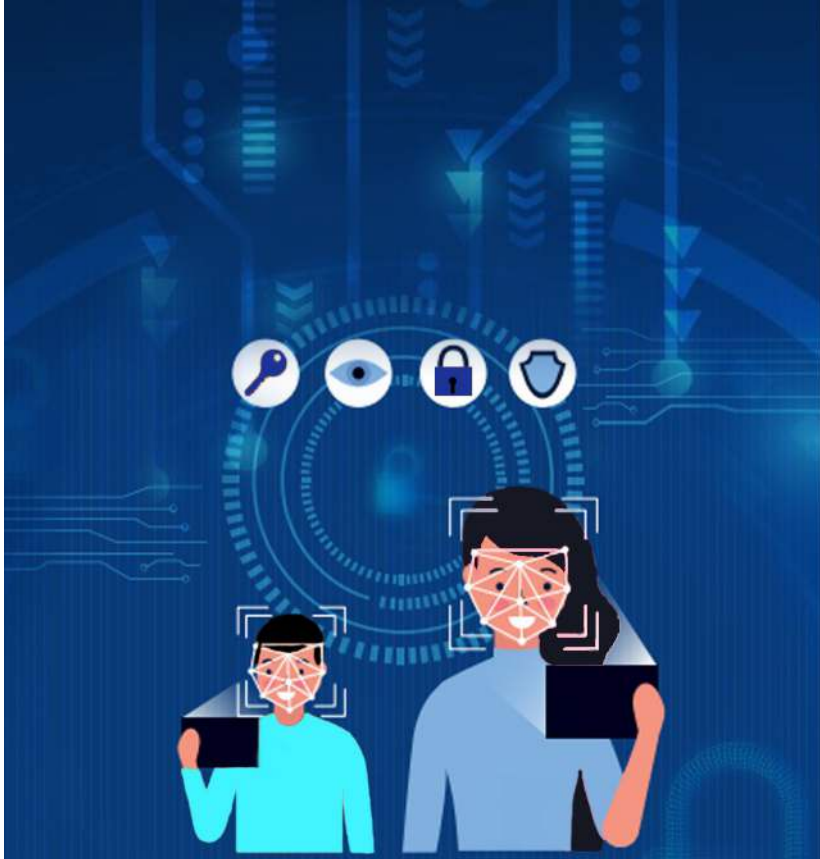
Enrolment under Cyber Gyan Project		
State	February 2022 - March 2025	January 2025 - March 2025
Uttar Pradesh	1261	165
Gujarat	472	66
Madhya Pradesh	459	187
Maharashtra	428	67
Bihar	427	187
Haryana	379	19
Tamil Nadu	349	48
Andhra Pradesh	284	68
Assam	274	29
Delhi	268	9
Kerala	232	29
Jammu and Kashmir	211	63
Manipur	186	9
Tripura	181	66
Punjab	156	40
Odisha	150	58
Telangana	149	86
Jharkhand	141	58
West Bengal	141	18
Chhattisgarh	131	10
Arunachal Pradesh	126	5
Rajasthan	125	35
Meghalaya	118	19
Uttarakhand	95	17
Mizoram	92	7
Karnataka	89	6
Himachal Pradesh	60	46
Puducherry	53	2
Sikkim	24	11
Nagaland	5	2
Goa	4	3
Grand Total	7070	1435



MAJOR PROJECT PERFORMANCE/ STATISTICS

INFORMATION SECURITY EDUCATION AND AWARENESS (ISEA) PROJECT PHASE –III

Information Security Education and Awareness (ISEA) Project Phase –III		
ISEA Activities	**January 2024 to March 2025**	**January 2025- March 2025**
	Total number of candidates	**Total number of candidates**
Generating highly skilled & certified Cyber Security Professionals - CISOs	Under CISO component of ISEA Project, conducted 13 Certificate trainings covering 407 CISOs/Dy. CISOs/Associate team of CISOs across India covering PSUs, Government, IT/ITES and Pvt sectors.	• C-DAC Hyderabad in association with Indian Computer Emergency Response Team (CERT-In) organized a 4-day training and certification programme on "Level 1 Training on "Cyber Security for Banking, Financial Services & Insurance Sector" during January 2025 at C-DAC Hyderabad Campus. This initiative was part of the NAAT audit and assessment, as well as the "Generating Highly Skilled & Certified Cyber Security Professionals (CISOs)" programme. 33 CISO team members/officers participated from various organisations. • A four-day training and certification programme on "Sector Specific Operational Technology (OT)/Industrial Control System (ICS) Security – Level 2" was conducted during January 2025 as part of "Generating Highly Skilled & Certified Cyber Security Professionals (CISOs)". • A four-day Training and Certification programme on "Sector Specific Telecom Security – Level 1" was conducted during February 2025 at Cert-In, New Delhi as part of "Generating Highly Skilled & Certified Cyber Security Professionals (CISOs)".
Academic and Innovation Activities	11,341 candidates trained/ undergoing training in various formal/ non-formal courses, short-term programs and innovation activities by 50 institutions.	5 Faculty Development Programs, 3 Short term programs, 10 Bootcamps and 3 National Workshops conducted by various academic institutions under the project.
Cyber Aware Digital Naagriks (Mass Awareness) • Cyber Hygiene, Security & Privacy • Role based awareness, progression pathways • Mass Awareness	ISEA Phase –III details up to March 2025 As part of "National Awareness Campaign on Information Security Education and Awareness (ISEA) Program – Phase III a total of – 2070 Awareness workshops / Training were organized by covering 4,67,413 participants	As part of "Cyber Aware Digital Naagrik (Mass Awareness Program) as part of Information Security Education and Awareness (ISEA) Program – Phase III a total of 1575 Awareness workshops / Training were organized by covering 3,13,400 participants from January to March 2025.



CYBER GYAAN

MAJOR PROJECT PERFORMANCE/ STATISTICS

SWAYAAN: CAPACITY BUILDING FOR HUMAN RESOURCE DEVELOPMENT IN UNMANNED AIRCRAFT SYSTEM

Project 'SwaYaan: Capacity Building for Human Resource Development in Unmanned Aircraft System' is led by C-DAC Hyderabad and IIITDM Kurnool as the Programme Management Unit (PMU) to develop a UAS/Drone Ecosystem across the Nation. The project is implemented in a hub-and-spoke model through 30 institutions including IISc Bangalore, IITs, IIITs, NITs, CDAC, and NIELIT Centres. Under the project, the overall target is to train 45,000+ candidates through various Formal, Non-Formal programs and Research Program such as MTech in UAS/Drones, Minor degree/Retrofitting courses in UAS/Drones, PG Diploma Program, Short term Skilling Courses, Innovation Challenge, Bootcamps, POC, National Workshops, International Conference, Open Online Courses, IPR (Paper and Patents) creation, etc. over a period of 5 Years.

Till 1st Quarter of 2025, a total of 607 activities have been conducted across India under various academic programs, research and innovation initiatives, training sessions, workshops, and other knowledge-sharing efforts. These initiatives have engaged 17,076 participants, collectively accelerating the nation's journey towards becoming a Global Drone Hub by 2030.

Program Name	Activity: 2022-2025			Participants: 2022-2025		
	January 2022 – December 2024	January 2025- March 2025	Total	January 2022 – December 2024	January 2025- March 2025	Total
FDP	19	2	**21**	473	51	**524**
Workshop	9	0	**9**	689	0	**689**
Bootcamp	305	48	**353**	11400	2045	**13445**
PG-Diploma	6	0	**6**	25	0	**25**
POC	80	37	**117**	414	233	**647**
M-Tech	1	0	**1**	23	0	**23**
Minor Degree	4	1	**5**	96	12	**108**
Retrofitting Electives	52	9	**61**	1213	291	**1504**
IPR-Paper	22	8	**30**	74	26	**100**
IPR-Patent	3	1	**4**	10	1	**11**
Total	**501**	**106**	**607**	**14417**	**2659**	**17076**

MAJOR PROJECT PERFORMANCE/ STATISTICS

SWAYAAN: CAPACITY BUILDING FOR HUMAN RESOURCE DEVELOPMENT IN UNMANNED AIRCRAFT SYSTEM

January 2025 – March 2025 Progress

Overall Progress

- For the 1st Quarter of 2025, SwaYaan conducted 88 Activities across 2401 Beneficiaries under 10 category of Programs

Research & Innovation

- Launched India's largest 'National Innovation Challenge for Drone Application and Research (NIDAR)'on 18th March 2025
- 37 Proof-of-Conceptes by 27 Centres have been approved with 233 Beneficiaries.
- IPR-8 Paper Publications and 1 Patent filed benefiting 27 Participants

Academic Activities

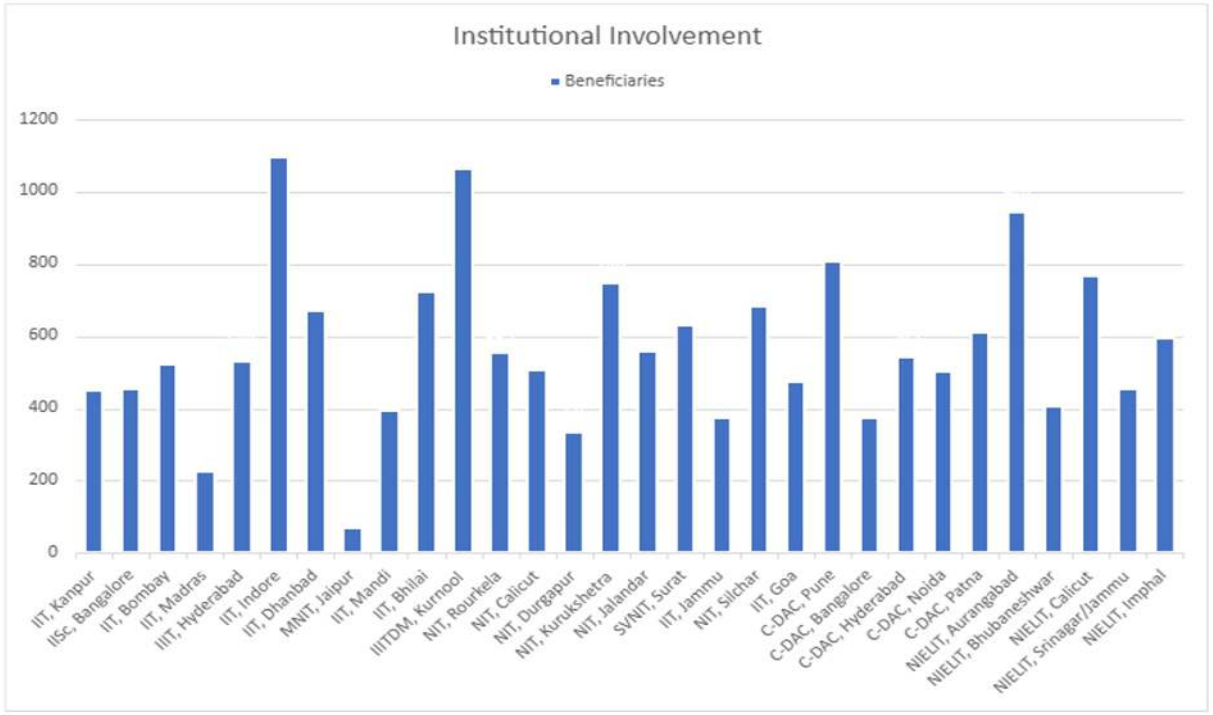
- 1 minor Degree on"Unmanned Aerial Systems and Applications" has been launched with 12 Beneficiaries
- 9 Retrofitting Electives have been launched with 291 Beneficiaries.

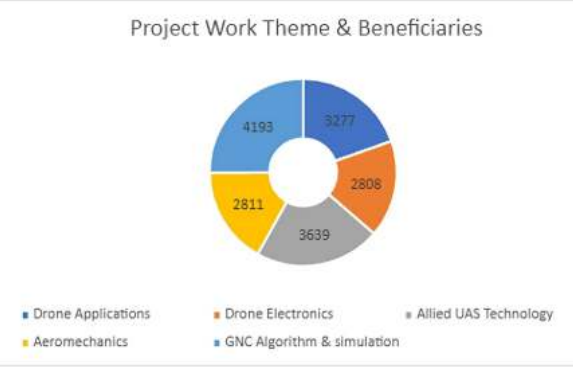
Training & Skilling

- 48 Bootcamps in Drone/UAS conducted by 15 Institutes marking participation by 2024 students
- Launch of new Job Role based course on Junior Engineer Drone (R&D) by Electronics Sector Skills Council of India on 25 th March 2025 at Noida and Bhopal Centers
- 2 Faculty Development Programms have been organized by 2 institutions with 51 Participants

MAJOR PROJECT PERFORMANCE/ STATISTICS

SWAYAAN: CAPACITY BUILDING FOR HUMAN RESOURCE DEVELOPMENT IN UNMANNED AIRCRAFT SYSTEM





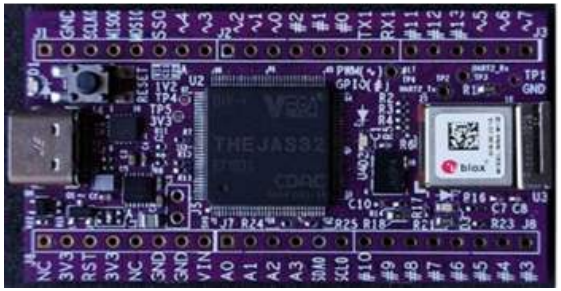
Work Theme	Beneficiaries
Drone Applications	3277
Drone Electronics	2808
Allied UAS Technology	3639
Aeromechanics	2811
GNC Algorithm & simulation	4193

TECH ROLLOUTS

SYSTEM/ PRODUCT/ SERVICES LAUNCH/ RELEASE

TECH ROLLOUTS

LAUNCH OF ARIES ECO AND NOVA BOARDS BY HON'BLE MINISTER OF E&T



ARIES Nova

ARIES Eco

Shri Ashwini Vaishnaw, Hon'ble Minister of Railways; Information and Broadcasting; and Electronics and Information Technology launched ARIES Eco and Nova boards based on indigenous THEJAS32 SoC ASIC developed as part of DIR-V program on January 11, 2025 at C-DAC Pune. ARIES ECO v1.0 is a development platform based on THEAJS32 ASIC which operates at a frequency of 100MHz. ARIES NOVA v1.0 is a comprehensive, robust indigenous hardware platform based on THEJAS32 SoC which includes VEGA ET1031 Microprocessor; is targeted to facilitate learning and development of Internet of Things (IoT) applications.

TECH ROLLOUTS

LAUNCH OF AGRIGLAMS

AgriGLAMS, a Gamified Learning Assessment and Management System for agricultural science, is an innovative online platform designed to enhance agricultural learning through interactive quizzes and competitions. AgriGLAMS is launched by Shri Arif Mohammed Khan, Hon'ble Governor of Bihar in Kisan Mela 2025 at BAU Sabour on March 11, 2025.

TECH ROLLOUTS

LAUNCH OF KANTHASTH 3.0 BAHUBHASHI

Kanthasth 3.0 Bahubhashi, a multilingual translation software, was unveiled at the Joint Regional Official Language Conference in Guwahati on March 5th, 2025. This alpha version, launched by Assam Chief Minister Dr. Himanta Biswa Sarma, Union Minister of State for Home Affairs Shri. Nityanand Rai, and Members of Parliament Shri. Dilip Saikia and Smt. Bijuli Kalita Medhi. Kanthasth 3.0 Bahubhashi is developed for the Bhartiya Bhasha Anubhag, this software is a significant step toward promoting Indian languages and enhancing translation efficiency.

INTERNATIONAL OUTREACH

INTERNATIONAL OUTREACH

HANDING OVER OF CESDT PHNOM PENH TO GOVERNMENT OF CAMBODIAN

Centre of Excellence in Software Development & Training (CESDT) in Phnom Penh was successfully handed over to Government of Cambodian on January 15, 2025. CESDT was established in Nov 2018 with the creation of state-of-the-art IT Infrastructure and supply of course material and reference books.

LRIT TRAINING FOR FRIENDLY FOREIGN COUNTRIES

A training session to demonstrate the capabilities and features of Long Range Identification and Tracking (LRIT) System, a National Critical Infrastructure implemented and managed by C-DAC Mumbai, was conducted for Defence Personnel from eight Friendly Foreign Countries (FFCs) namely Bangladesh, Brunei, Maldives, Mauritius, Myanmar, Oman, Seychelles and Sri Lanka at LRIT National Data Centre in Sagar-Manthan: Mercantile Marine Domain Awareness Centre (MMDAC) Facility, Nav Bhavan, Mumbai on February 22, 2025.

EVENTS

EVENT

Analog & Digital Hackathons under C2S – Results Declaration

The 100-hour Analog and Digital hackathons, held from March 16-20, 2025, brought together some of India's brightest minds to develop and implement innovative VLSI designs. The Grand Finale and award ceremony was marked by the virtual announcement of winners by Hon'ble Minister Shri Ashwini Vaishnaw, along with Secretary Shri Krishnan, Additional Secretary Shri Abhishek Singh, Group Coordinator Smt Sunita Verma, MeitY, Director General, C-DAC and Executive Director, C-DAC Bangalore.

EVENT

Indian Web Browser Development Challenge (IWBDC) – Results Declaration

The result declaration ceremony of the Indian Web Browser Development Challenge (IWBDC) was organised on March 20, 2025 at Rail Bhavan, New Delhi in the august presence of Honourable Minister for electronics and information technology, Shri Ashwini Vaishnaw. The Honourable Minister declared the results of the challenge before the media.

EVENT

National Workshop on Ransomware and Digital Infrastructure Protection (NWRDIP)

The National Workshop on Ransomware and Digital Infrastructure Protection (NWRDIP-2025) was organized by C-DAC Patna at Indira Gandhi Planetarium, Patna. It was honored by esteemed dignitaries, Prof. Dr. Bindey Kumar (Director, IGIMS) as Chief Guest, along with Shri Rakesh Rathi, IPS (IG Cyber, EOU, Bihar Police), Shri Sanjay Kumar, IPS (DIG, Cyber, EOU), Shri Ajay Kumar (State Informatics Officer, NIC), Shri Aditya Kumar Sinha (Director, C-DAC Patna), Shri Subrata Saha Roy (Commandant, SSB), Shri Sanjeev Kumar (DGM, RBI), and Shri Pankaj Prasad (Manager, RBI).

EVENT

National Symposium on Developing Innovation, Incubation and IPR Ecosystem (NSDIIIE)

The National Workshop on Ransomware and Digital Infrastructure Protection (NWRDIP-2025) was organized by C-DAC Patna on March 08, 2025, bringing together policymakers, industry leaders, academicians, and legal experts to deliberate on strengthening India's IPR and innovation landscape. It was honored by esteemed dignitaries, Hon'ble Minister of Industries, Government of Bihar, Shri Nitish Mishra as Chief Guest, along with Shri Rajesh Singh (Joint Secretary & Financial Advisor, MeitY, Govt. of India), Shri Vijay Prakash (Retd. IAS, Chairman & CEO, AIC-Bihar Vidyapeeth), Shri Aditya Kumar Sinha (Director, C-DAC Patna), Prof. (Dr.) Rana Singh (Director, Chandragupt Institute of Management Patna), Prof. (Dr.) Nitin Kumar Puri (Executive Director, NIELIT Patna), and Advocate Vedant Pujari (Director & Managing Partner, Acures IP Care).

EVENT

TechWeave – 2025, ICT for Livelihood

The two-day workshop, "TechWeave – 2025, ICT for Livelihood," designed to enhance the entrepreneurial and employment prospects of weavers and artisans in the Bodoland Territorial Council (BTC), Assam, was successfully conducted by C-DAC Kolkata. Funded by MeitY, Govt. of India, this event, part of the "Capacity Building Programme using ICT Tools & Technology to Enhance Livelihood of Weavers/Artisans of Bodoland Territorial Council (BTC), Assam" project, took place at the Handloom Training Institute, Mushalpur, Baksa, Assam, on February 27-28, 2025. The valedictory session was graced by Ms. Tulika Pandey, Scientist G & GC (HRD), MeitY, Shri. Gautam Das, DC, Baksa, Shri. S. Bandyopadhyay, Zonal Director (E), WSC, Ministry of Textiles, Shri. D. N. Hazarika, Addl. Secretary, Govt. of Assam, and Dr. Ch. A S Murty, Scientist G & Centre Head, C-DAC Kolkata.

EVENT

Workshop on Seismic Modelling and Migration using SeisRTM

A three-day workshop on "Seismic Modeling and Migration using SeisRTM" was conducted at IIT (ISM), Dhanbad during February 8-10, 2025. SeisRTM is an advanced and highly customizable Reverse Time Migration (RTM) software designed for efficient seismic imaging, by C-DAC Pune in collaboration with IIT Roorkee and ONGC as part of India's National Supercomputing Mission (NSM) under MeitY. The workshop was jointly organised by Seismic Data Processing (SDP), C-DAC Pune; Dept. of Applied Geophysics, IIT (ISM) Dhanbad and Dept. of Earth Sciences, IIT Roorkee.

आईआईटी-आईएसएम में सीस्मिक, मॉडलिंग और माइग्रेशन की तीन दिवसीय कार्यशाला आयोजित

स्वदेश संवाददाता

धनबाद : शनिवार को आईआईटी आईएसएम धनबाद के न्यू लेक्चर हॉल परिसर के लैब 3 में 140 से अधिक छात्रों ने सीस्मिक मॉडलिंग और माइग्रेशन पर तीन दिवसीय कार्यशाला के उद्घाटन सत्र में भाग लिया। यह कार्यशाला आईआईटी आईएसएम के एप्लाइड जियोफिजिक्स विभाग द्वारा आईआईटी रुड़की के अर्थ साइंसेज विभाग और सी-डैक पुणे के सीस्मिक डेटा प्रोसेसिंग विभाग के सहयोग से आयोजित की गई है। कार्यशाला के पहले दिन में प्रतिभागियों को बुनियादी एलआईएनयूएक्स और एसएलयूआरएम कमांड्स, 2डी मॉडल जियोमेट्री

क्रिएशन, और 2डी आइसोट्रॉपिक मॉडलिंग का उपयोग करके सीस्मिक डेटा उत्पन्न करने जैसे बुनियादी विषयों से परिचित कराया गया। इस क्षेत्र के विशेषज्ञों ने अपने विचार साझा किए, जिनमें सी-डैक पुणे की वैज्ञानिक रिचा रस्तोगी द्वारा सीस्मिक मॉडलिंग पर एक महत्वपूर्ण प्रस्तुति दी गई। सी-डैक पुणे की सीनियर प्रोजेक्ट इंजीनियर, नीटू मंगलाथ ने एसइआईएस आरटीएम सॉफ्टवेयर पर एक सत्र का संचालन किया।कार्यक्रम के एक हिस्से के रूप में, मुख्य अतिथि, प्रोफेसर धीरज कुमार, आईआईटी आईएसएम के उप निदेशक ने SeisRTM सॉफ्टवेयर के व्यापक अनुप्रयोगों पर जोर दिया। उन्होंने कहा कि जबकि कार्यशाला मुख्य रूप से इसका उपयोग सिस्मोलॉजी में कर रही है, इसका खनिज अन्वेषण, खनिज प्रसंस्करण, संसाधन आरक्षित अनुमान और खनिज डीपोसीटोंज की वसूली में महत्वपूर्ण महत्व है। प्रोफेसर कुमार ने कहा दुनिया अब खनिज अन्वेषण में गैर-विनाशकारी प्रौद्योगिकियों का पता लगाने और मौजूदा भंडारों में मूल्य जोड़ने के लिए भूभौतिकीविदों पर अधिक निर्भर हो रही है। कार्यशाला 9 फरवरी को आईआईटी रुड़की के अर्थ साइंसेज विभाग के प्रमुख प्रोफेसर आनंद जोशी द्वारा आरटीएम के सैद्धांतिक पहलुओं पर एक प्रस्तुति के साथ जारी रहेगी। प्रतिभागी हाथों-हाथ सत्रों में भाग लेंगे, जिसमें पहले दिन उत्पन्न डेटा का उपयोग करके सीस्मिक माइग्रेशन और एसइजीवाई डेटा और तीसरी पार्टी के सीस्मिक डेटा का उपयोग करके सीस्मिक माइग्रेशन पर ध्यान केंद्रित किया जाएगा।

EVENT

Awareness Programme on Information Security for BSF Officials

A two-day training programme on "Information Security and Emerging Technologies" was conducted by the C-DAC Silchar for Border Security Force (BSF) officials from the Mizoram and Cachar Frontier headquarters. Held on January 22 – 23, 2025, the programme was part of the EPPGO project, which focuses on providing IT and cybersecurity training to police and government personnel in the North-East region. The training programme commenced with an inaugural session featuring Shri Lakhminder Gill, Deputy Inspector General of the BSF's M&C Frontier Headquarters, as the chief guest.

EVENT

Workshop for Rajasthan Government Departments

C-DAC Mumbai organized a one-day workshop on “Digital Governance with Emerging Technologies” in Jaipur on February 12, 2025 for all the government departments of Rajasthan. Mrs. Archana Singh, IAS, Secretary and Commissioner, Department of Information Technology & Communications (DOIT&C), joined the workshop as chief guest, exploring emerging technology trends for the Rajasthan government and potential collaborations with C-DAC Mumbai. The workshop was attended by over 120 participants from various government departments including DOIT&C, Horticulture Dept, SCRB, Agriculture Dept, RISL RajCOMP Info Service Ltd, Jaipur Vidyut Vitran Nigam Ltd., etc.

BACKEND
SQUAD

BACKEND SQUAD

CISO DESK

- The implementation of C-DACSIEM has been successfully completed across all 12 C-DAC centres.
- Actions have been taken for the various threat incidents reported during the period.
- Safer Internet Day was celebrated at C-DAC centers in the month of February 2025.
- More than four training/Awareness/ Lectures/ Webinars etc. were conducted during the period including session on Malware Decoded: Impact, Trends and Prevention, Navigating the Digital Highway: Safeguarding Your Online Journey, Awareness on IoT Security, etc.

CIO DESK

The CIO & NIO teams have been actively working to streamline processes and enhance service delivery for Shared IT Services within C-DAC. Key initiatives include the deployment of the Bitrix24 Project Management Tool, which is now hosted on the C-DAC Thiruvananthapuram Server with access granted across PAN C-DAC. The team is also progressing with C-DAC's email migration to the NIC Server and the on-premises SSO setup. The Helpdesk Management System has been integrated with the Asset Management service, while the Visitor Management System is undergoing LDAP integration and security testing. Asset Management updates are ongoing across centres, managed by the C-DAC Bangalore team. For Shared IT Services 1.0, a draft SOP and escalation matrix have been prepared, with further evaluations in progress. Additionally, efforts are being made to develop and deploy a Virtual Desktop Infrastructure (VDI) solution.

सी डैक
CDAC

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● बेंगलुरू ● चेन्नई ● हैदराबाद ● कोलकाता ● मोहाली ● मुंबई ● नई दिल्ली ● नॉएडा ● नॉर्थ ईस्ट (सिलचर) ● पटना ● पुणे ● तिरुवनंतपुरम
● Bengaluru ● Chennai ● Hyderabad ● Kolkata ● Mohali ● Mumbai ● New Delhi ● Noida ● North East (Silchar) ● Patna ● Pune ● Thiruvananthapuram

Branding & Communication/Corporate R&D/2025