Category No.5: C-DAC, Bangalore, Project Engineer –VLSI Design (Logic Design)

Post:	Project Engineer –VLSI Design (Logic Design)
Post Code:	PE- 04/LD
No. of Posts	2
Duration of the position	Three Years
Educational Qualification	• Full time 1st Class B.E/ B. Tech in Electronics & Communication / Telecommunication / Electronics or Equivalent with minimum 2 years of relevant post qualification work experience. **OR** • Full time 1st Class B.E/ B. Tech in Electronics & Communication / Telecommunication / Electronics or Equivalent **AND** Full time 1st class M.E/M. Tech in Micro-Electronics/ VLSI Design/ Electronics or equivalent plus at least 1 year of relevant post qualification work experience.
Mandatory Experience (in one or more topics)	• Hand-on experience in RTL simulation, verification and modeling using VHDL/ Verilog/ System Verilog. • Knowledge of Digital IC Design (Simulation/ Synthesis [ASIC/ FPGA]/ Static Timing Analysis/ Logic Equivalence Check/ Back-Annotation/ DFT). • Experience in prototyping the developed IP cores on FPGAs. • Fundamentals of Computer Architecture, Arithmetic Units Design, Bus protocols Architecture and Design, Memory Controllers Design and SoC Design.
Other Skills and Qualities	• Basic knowledge of C & Assembly level programming and scripting. • Good debugging, problem solving/ analytical skills. • Good interpersonal skills and ability to work in a team.
Mode of selection	Written Test and Interview
Monthly Consolidated salary	Rs. 31,000 /- plus based on the post qualification relevant experience
Maximum Age	30 years