

**Category No.2: C-DAC, Bangalore, Project Manager –VLSI Design**

Post:	Project Manager – VLSI Design
Post Code:	PM- 01/VLSI
No. of Post	1
Duration of the position	Three Years
Educational Qualification	<ul style="list-style-type: none"> <li>• Full time 1<sup>st</sup> Class B.E/ B. Tech in Electronics &amp; Communication / Telecommunication / Electronics or Equivalent with at least 11 years of relevant post qualification work experience.</li> </ul> <p style="text-align: center;"><b>OR</b></p> <ul style="list-style-type: none"> <li>• Full time 1<sup>st</sup> Class M.E/ M. Tech in VLSI Design / Microelectronics/ Electronics or Equivalent with at least 7 years of relevant post qualification work experience.</li> </ul> <p style="text-align: center;"><b>OR</b></p> <ul style="list-style-type: none"> <li>• Ph.D in VLSI Design / Microelectronics / Electronics with at least 4 years of post-qualification work experience</li> </ul>
Mandatory Experience (in one or more topics)	<ul style="list-style-type: none"> <li>• Hand-on experience in RTL simulation, verification and modeling using VHDL/ Verilog/ System Verilog.</li> <li>• Knowledge of Digital IC Design (Simulation/ Synthesis [ASIC/ FPGA])/ Static Timing Analysis/ Logic Equivalence Check/ Back-Annotation/ DFT).</li> <li>• Experience in prototyping the developed IP cores on FPGAs.</li> <li>• Hand-on experience in FPGA/ASIC Design tool sets.</li> <li>• IP core design for Arithmetic Units, Bus protocols, Memory Controllers and SoC design.</li> <li>• PCIe, DDR3/4, 1G and 10G Ethernet based design experience.</li> <li>• Microblaze, PPC or ARM SoC etc. based FPGA design projects</li> <li>• Coordinated teams for the execution of FPGA/ASIC projects</li> <li>• Skilled to develop a detailed project plan to monitor and track progress</li> <li>• Experience in Physical Design handling Netlist to GDSII flow.</li> <li>• Experience in ASIC Synthesis, Floor Planning, Placement Optimizations, CTS, Routing and Timing Closure of Full-Chip designs.</li> <li>• High Speed Serial Link design / simulation</li> <li>• Power and Interconnect network integrity and validation</li> </ul>
Other Skills and Qualities	<ul style="list-style-type: none"> <li>• Basic knowledge of scripting languages is desirable.</li> <li>• Good debugging, problem solving / analytical skills.</li> <li>• Good interpersonal skills and ability to handle teams.</li> </ul>
Mode of selection	Interview
Monthly Consolidated salary	Rs 64000 plus based on the post qualification relevant experience
Maximum Age	40 Years